Problem 2

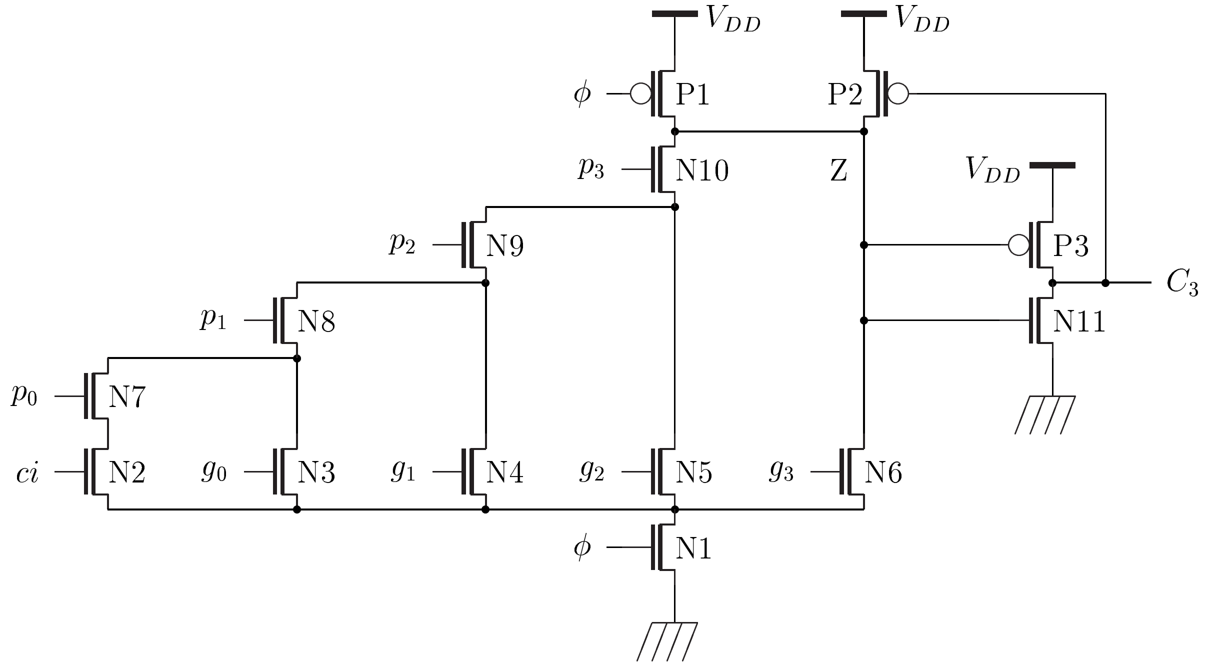

Figure 2: Transistor diagram of latched CMOS domino circuit

In this problem, the design of a latched CMOS domino circuit is discussed. The transistor diagram is shown in Figure 2.
The channel width of any transistor is 2.5μm. The minimum channel length is used for all transistors, except for transistor $P2$, which has a longer channel. The supply voltage is $V_{DD} = 3V$.

Question 2.1

Discuss, which matters must be considered in the design of the circuit in Figure 2.
Explain how to determine the length of transistor $P2$.
Specify the combination of input signals $(\phi, ci, p_0, p_1, p_2, p_3, g_0, g_1, g_2, g_3)$, which results in the worst case shift of the circuit.

Question 2.2

Determine the length of transistor $P2$. In the reply, body effects are disregarded.

Question 2.3

Draw a pull-up and pull-down graph for the internal node Z corresponding to the transistor diagram in Figure 2, in which both n-channel and p-channel areas are realized as single lines of diffusion.
Draw the layout of the circuit.

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Appendix 1: 1.0μm CMOS process parameters and design rules

Film thickness		
Gate oxide thickness	t_{ox}	200 Å
Field oxide thickness	t_F	5000 Å
Oxide thickness between poly and metal-1	t_{mp}	7000 Å
Oxide thickness between metal-1 and metal-2	t_{mm}	12000 Å
Thickness of polysilicon layer	t_p	4000 Å
Thickness of metal-1 layer	t_{m1}	6000 Å
Thickness of metal-2 layer	t_{m1}	10000 Å
Junction depth p^+/n^+ diffusion	x_j	4000 Å
Junction depth n-well diffusion	x_w	30000 Å
Depletion layer thickness pn junction	x_d	3000 Å
Depletion layer thickness under channel	x_k	3000 Å

Transistor parameters		
Current factor	KP_n	98
$[\mu A/V^2]$	KP_p	38
Threshold voltage	V_{tn0}	0.8
$[V]$	V_{tp0}	- 0.8
Body effect	γ_n	0.75
coefficient $[\sqrt{V}]$	γ_p	0.75
Bulk potential	ϕ_{bn}	0.37
$[V]$	ϕ_{bp}	- 0.37
Channel length	λ_n	0.01
modulation $[V^{-1}]$	λ_p	0.038

Capacitances		Area $fF/\mu m^2$		Perimeter $fF/\mu m$	
metal-2	to substrate	C_{m2}	0.017	C_{m2p}	0.052
metal-1	to substrate	C_{m1}	0.029	C_{m1p}	0.046
poly	to substrate	C_p	0.058	C_{pp}	0.055
n^+ diffusion (0V)	to substrate	C_{jn}	0.40	C_{jnp}	0.52
p^+ diffusion (0V)	to substrate	C_{jp}	0.62	C_{jpp}	0.87
gate capacitance		C_{ox}	1.95		—