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	FPGA	Digital biochip
Basic Devices Tiles	Transistors	Control electrodes
	Net Wires	Reservoirs
	Clock lines	Transparent cells
	RAM	Mixers
	Multiplexer	Transport bus
	CLBs	Optical detectors
Systems	Configured FPGA	Configured biochip















Problem Formula	ation			
Given				
Application: graph				
Biochip: array of electrodes				
Library of modules				
Determine				
Allocation of modules from modules library				
Binding of modules to operations in the graph				
Scheduling of operations				
Placement of modules on the array				
Such that				
the application execution time is minimized				
	22			































	Solution
Binding of modules to operations	Tabu Search
 Schedule of the operations Placement of modules performed inside scheduling 	List Scheduling
 Placement of the modules Free space manager based on [Bazargan et al 2000] that divides free space on the chip into overlapping rectangles 	
 Other solutions proposed in the literatur Integer Linear Programming Simulated Annealing 	re:
	38




































































outing-Based Synthesis (I	RBS) vs. to Moo	dule-Based Sy	nthesis (M
Application	Area	B	est
11		RBS	MBS
	8 × 9	68.43	72.94
In-vitro	8×8	68.87	82.12
(28 operations)	7×8	69.12	87.33
	11 × 11	113.63	184.06
Proteins	11×10	114.33	185.91
(103 operations)	10×10	115.65	208.90

73

Discussion Module-based vs. routing-based Module-based needs an extra routing step between the modules; Routing-based performs unified synthesis and routing Module-based wastes space: only one module-cell is used; Routing-based exploits better the application parallelism Module-based can contain the contamination to a fixed area; • We have extended routing-based to address contamination • Hybrid approaches are also possible Non-rectangular modules Droplet-aware module-based synthesis Area-constrained routing-based synthesis 74

































Time Cost for Control Path Design

- Part 1: time cost for the storage of the intermediate product droplet at the checkpoint (can be omitted)
- Part 2: time cost for transporting the intermediate product droplet to an on-chip detector (can be omitted)
- Part 3: time cost for error-detection
 - Typically 5 seconds for an LED-photodiode detector
 - Capacitive-sensing circuit operates at relatively high frequency (15 kHz)
- Part 4: time cost for implementing the re-execution subroutine
 - Sub-part 1: time cost for retrieving stored copy droplets and bringing to inputs of fluidic operations in the subroutine
 - Sub-part 2: time cost for re-executing the subroutine (e.g., operations O_1 and O_2 for checkpoint C_2)

91









Softwa	are fo	or Ro	llbac	k Recov	very
memory	ution sub	proutine		software in mi onds to a fragr	
Subprogram for checkpoint C_2	Address	Fluidic operation	Duration (seconds)	Resource	Module placement
	0083	<i>O</i> ₀	0-6	4-electrode mixer	(2,2)
	0084	<i>C</i> ₁	7-12	Detector 1	(1,1)
	0085	<i>O</i> ₁	13-21	2x3-array dilutor	(3,3)
	0086	<i>O</i> ₂	22-27	2x4-array dilutor	(2,4)
	0087	<i>C</i> ₂	28-33	Detector 1	(1,1)
	0088	<i>O</i> ₅	7-15	2x3-array dilutor	(5,6)
	0089	<i>C</i> ₃	16-21	Detector 2	(10,1)
	0090	<i>O</i> ₃	30-35	2x4-array dilutor	(6,2)
	0091	<i>O</i> ₄	36-42	4-electrode mixer	(4,6)





Control Software for Protein Assay

- Map control-path-based protein assay synthesis results to software program in micro-controller memory
- C_4 to C_7 are checkpoints for operations Dlt_4 to Dlt_7

Subprogram for	Address	Fluidic operation	Duration (seconds)	Resource	Module placement	
checkpoint C ₅	0011	Dlt ₄	46-53	4-electrode dilutor	(3,1)	
	0012	<i>C</i> ₄	54-59	Detector 1	(1,1)	
	0013	Dlt ₅	76-81	2x4-array dilutor	(5,3)	
	0014	<i>C</i> ₅	82-87	Detector 3	(5,1)	
	0015	Dlt ₆	56-61	2x4-array dilutor	(1,5)	
	0016	<i>C</i> ₆	62-67	Detector 1	(1,1)	
	0017	Dlt ₇	58-70	2x2-array dilutor	(5,3)	
	0018	C ₇	71-76	Detector 2	(1,10)	
	Software corresponding to the bioassay synthesis 99					



















