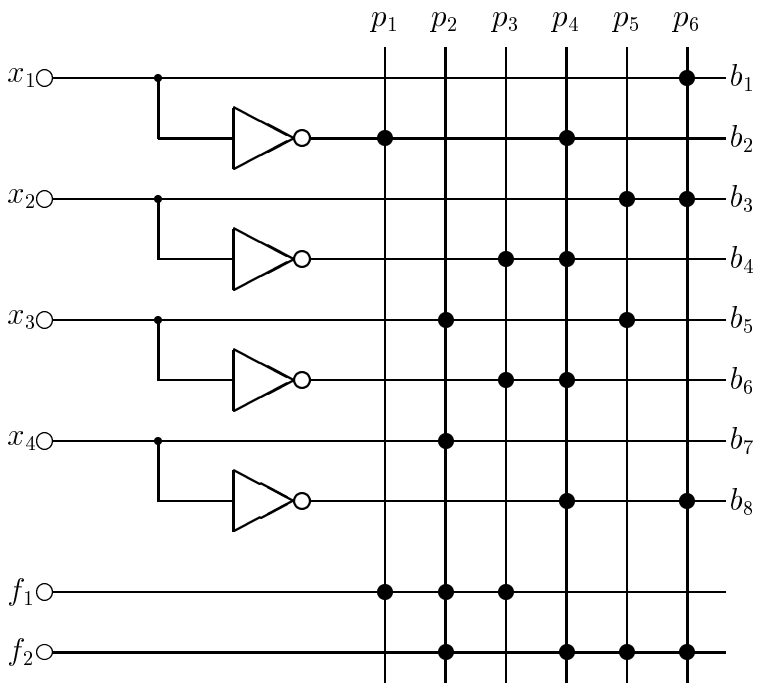
7 Test of Regular Structures

Problem 7.1: **PLA test.**

Prove that a missing crosspoint fault is equivalent to some stuck-at fault in the sum-of-product representation of a PLA.

Problem 7.2: **PLA test.**



For the PLA design shown above, construct the Karnaugh map for f_1 and f_2, and indicate the product terms implemented by the PLA for each of the following cases.

Question 1 The original PLA.

Question 2 A shrinkage fault caused by a connection between bit line b_1 and product line p_1.

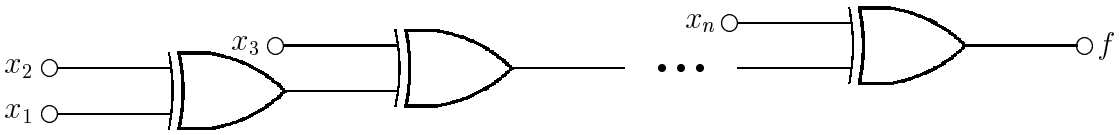
Question 3 A shrinkage fault caused by a connection between bit line b_6 and product line p_1.

Question 4 A growth fault caused by the missing connection between bit line b_1 and product line p_6.

Question 5 An appearance fault due to an extra connection between p_4 and f_1.

Question 6 A disappearance fault due to the missing connection between p_6 and f_2.

Problem 7.3: $\mathcal{C}$**-testability.**



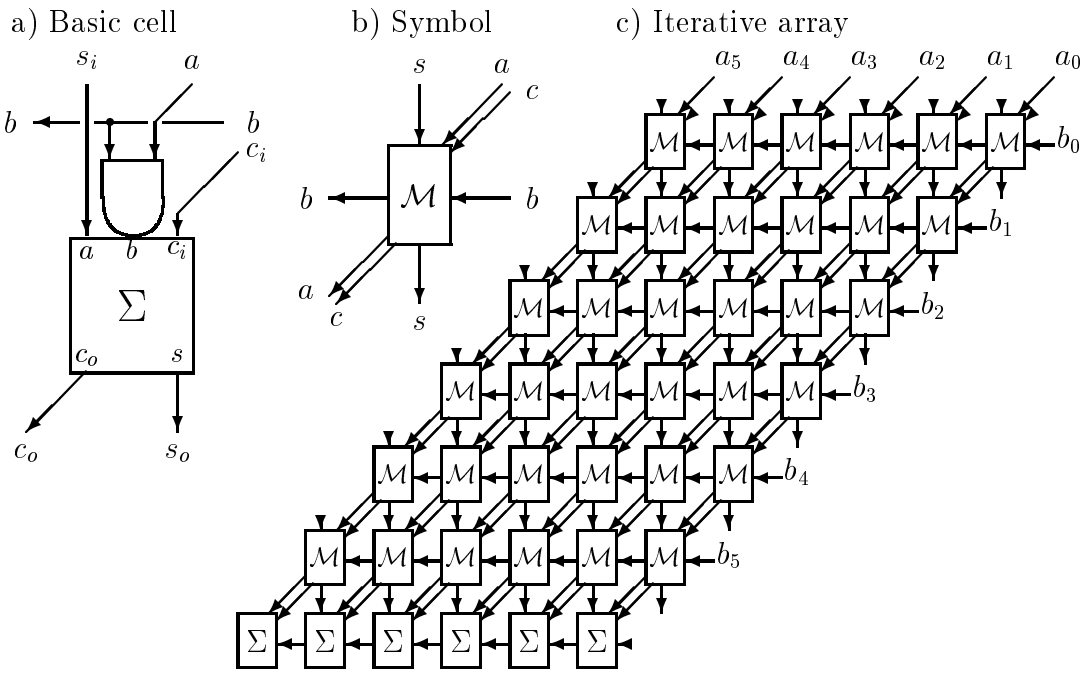
The circuit realizes the n-bit parity function. The basic cell implements the n-input exclusive-OR function.

Question 1 Use D-cubes to analyse fault propagation through the basic cell.

Question 2 Show that the iterative array is $\mathcal{C}$-testable with 4 test vectors.

Question 3 Determine all check points and generate a complete set of test vectors detecting all single stuck faults.

Problem 7.4: $\mathcal{C}$**-testability.**



Consider the iterative multiplier construction shown above.

Question 1 Explain how the multiplier works, and determine the boundary conditions of the array.

Question 2 Discuss controllability and observability of the array. Further, determine whether all cell states are used in normal, fault-free operation.

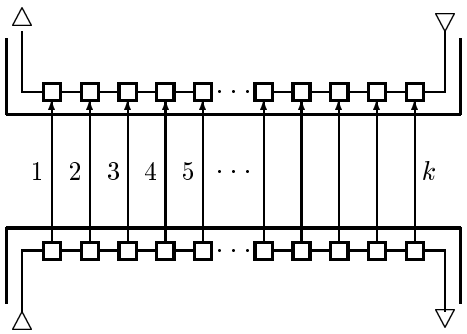
Question 3 Analyse fault propagation through the array.

Question 4 Determine the constraint graphs for the array and discuss, whether the array is $\mathcal{C}$-testable.

Question 5 Show a simple design change to the basic cell, that will make the entire array $\mathcal{C}$-testable. How many vectors are used for the test ?

8 Board-Level Testability

Problem 8.1: **Interconnect test.**



In the figure above, a number of nets connects two ICs both equipped with boundary scan chains.

Question 1 Determine a minimal set of test patterns that
a) detects any interconnect open, where opens are modeled as nets stuck-at-1 or stuck-at-0,
b) detects any short between two nets. Shorts are modeled as (symmetrical) wired-AND or wired-OR connections.

Question 2 Calculate the number of test patterns for a printed circuit board containing 2,500 nets.

Question 3 Assume the following values are applied to and received at nets 1 through 4:

$$\left.\begin{array}{ccc} 0 & 0 & 1 \\ 0 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 0 \end{array}\right\} \longmapsto \left\{\begin{array}{ccc} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{array}\right.$$

Discuss how the test response may be interpreted and determine extra test patterns necessary for fault location.

Problem 8.2: **Static test vector compaction.**

9 Fault-Tolerant Systems

Problem 9.1: Transparent RAM test.

Periodic on-line testing means activating a test phase periodically, during which a specific set of test patterns are run. Typically implemented using built-in self test, the problem of periodic on-line test is loss of circuit state, thus application execution context.

For random access memories, standard test patterns may be applied, but the previous contents of the RAM is lost during test. One such standard RAM test sequence is the March-C test:

$$\Updownarrow (w0) \Uparrow (r0w1) \Uparrow (r1w0) \Downarrow (r0w1) \Downarrow (r1w0) \Updownarrow (r0)$$

Convert the March-C test into a *transparent* RAM test, i.e. the original contents of the error-free RAM is restored after the test sequence.

10 Test Pattern Compaction

Problem 10.1: Test vector compatibility.

Show that if two input vectors of the same, combinational circuit are compatible, then their corresponding output vectors are also compatible.

Problem 10.2: Static test vector compaction.

Merge the following test patterns into a minimal number of test vectors:

(x101xx1)	(000xxxx)	(00xxx1x)	(x1xx0xx)
(1x0x10x)	(xx0x000)	(xxx011x)	(xx1x0xx)
(1x01xxx)	(x0xx00x)	(0x1x1xx)	(xx11xxx)

Problem 10.3: Static test set compaction.

Merge the following three sequences of test patterns into a single sequence:

s_1	(000xx0)	s_2	(x0xx10)	s_3	(001011)
	(x0x11x)		(x1x1x1)		(0x0110)
	(11xx01)		(x11001)		(111xx0)
	(0xx0x1)		(000x10)		(0xxx10)
					(000010)

Problem 10.4: Dynamic test compaction.

Assume that during dynamic compaction an attempt to create a test for a fault is unsuccessful. Under what conditions would another attempt be made to create a test for the fault?

12 Test Economy

Problem 12.1: 'Law of 10'.

Given a printed circuit board (PCB) containing 100 ICs. For each of two alternative test strategies, test sequences are found achieving 100 percent fault coverage.

Strategy 1. Each IC is individually tested prior to assembly, thus assembled boards contain only good ICs. The costs of testing any IC amounts to Ecu 1.

Strategy 2. No ICs are tested before assembly, and test and fault location are performed at board level. The costs of locating a faulty IC on a PCB amounts to Ecu 10.

Determine the level of IC yield at which it is cost effective to switch from using Strategy 1 to using Strategy 2.

Problem 12.2: Mixed test strategies.

At the end of an assembly line the manufactured printed circuit boards are put through a test. The yield of the assembly line is above 50 %. The objective of the test is a 0 % defect level in the shipped products. Faulty boards are diagnosed and returned to production for repair.

To this end, the assembly line may dispose of two different testers, a functional tester (FCT) and an in-circuit tester (ICT). The two testers are characterised by the following:

	FCT	*ICT*
Fault coverage	100 %	80 %
Handling	$\frac{1}{2}$ minute	$\frac{1}{2}$ minute
Testing	$\frac{1}{2}$ minute	1 minute
Fault diagnosis	6 minutes	1 minute

Question 1 Calculate the number of boards tested per hour (throughput) by each of the two testers as a function of the incoming defect level.

Question 2 Assuming the yield of the assembly line is 50 %, devise an effective test strategy and calculate the throughput.

Question 3 Assuming the yield of the assembly line is 95 %, devise an effective test strategy and calculate the throughput.