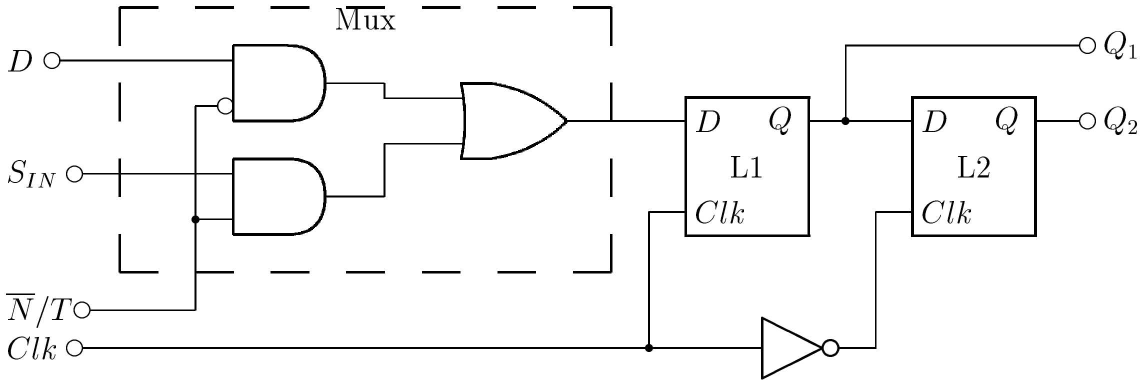
6 Design for Testability

Problem 6.1: Ad-hoc design rules.



A scan register is implemented using *multiplexed data flip-flops* as shown in the figure.

Show that clock skew may lead to erroneous operation during shifting.

Problem 6.2: LSSD design.

A double-latch LSSD configuration consists of 100 SRLs.

If the test requires 1000 test vectors, how many clock cycles are then required to test this circuit ?

Problem 6.3: LSSD design.

Consider a single-latch LSSD design and determine the best way to organize the testing of the logic blocks N_1 and N_2 to minimize test time for the two cases discussed below, when the number of secondary outputs of N_1 and N_2 are 10 and 30 respectively.

Question 1 Assume N_1 requires 10 test vectors, and N_2 requires 30.

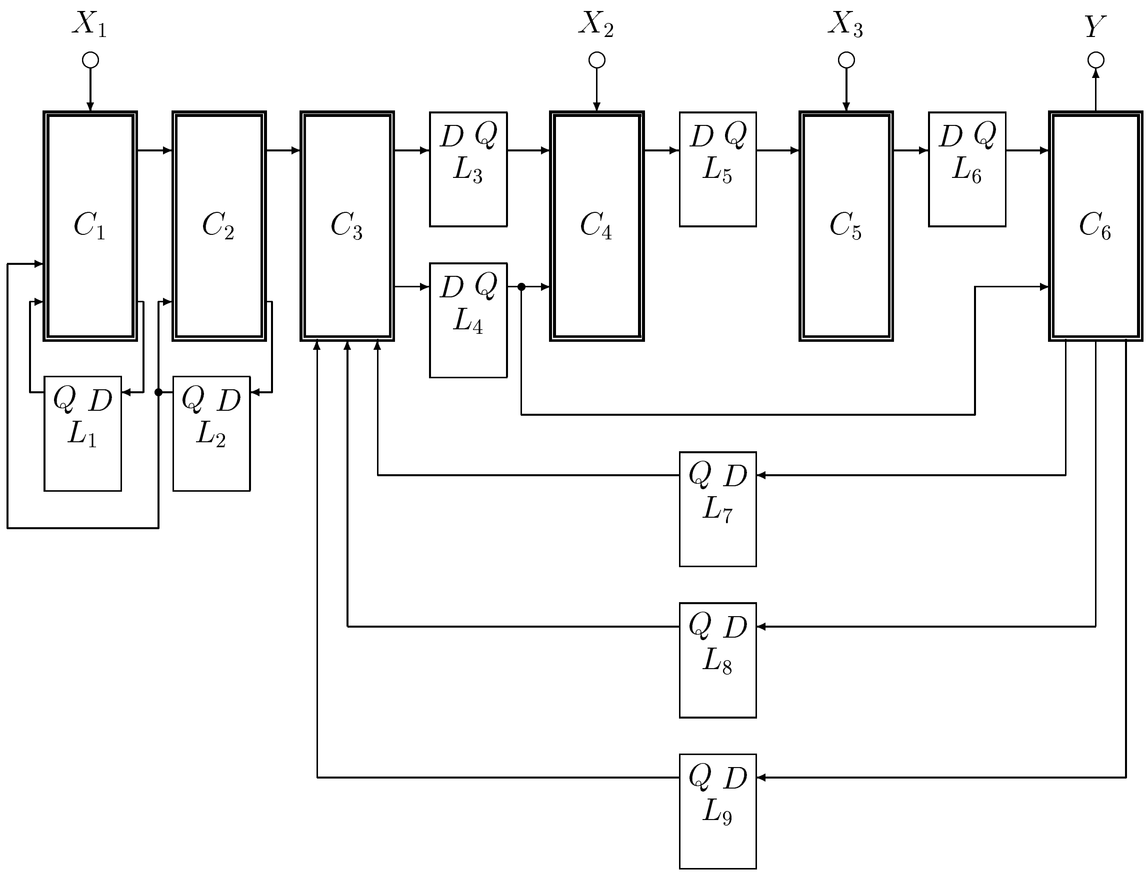
Question 2 Assume N_1 requires 30 test vectors, and N_2 requires 10.

Problem 6.4: Partial scan design.

Argue for or against the following proposition:

Randomly selecting a subset of flip-flops to be made part of a scan path in a partial scan design will reduce ATG cost compared to a nonscan design.

<u>Problem 6.5:</u> **Partial scan design.**



Partial scan is implemented in the circuit above. Thus, a few, not all, of the flip-flops will be made part of the scan path.

Discuss which FFs are essential to put into the scan path and identify a minimum number and a configuration of such flip-flops.

<u>Problem 6.6:</u> **Generator polynomials.**

The polynomial $x^{16} + x^{12} + x^5 + 1$ is studied in detail.

Question 1 Show that the polynomial detects all single and double errors.

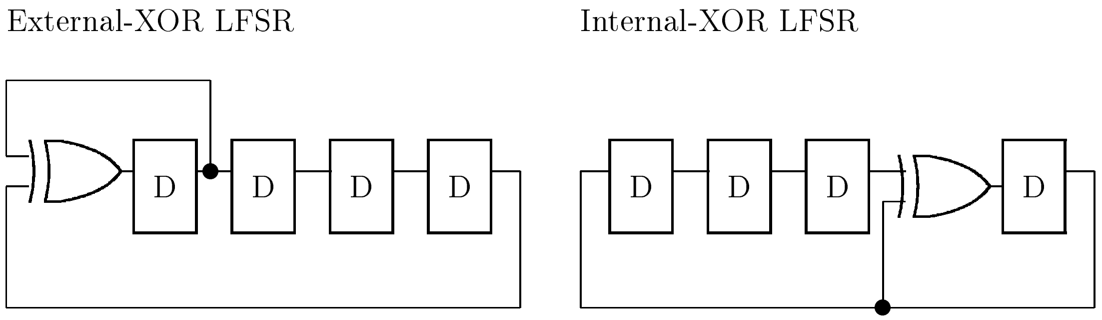
Question 2 Show that the polynomial detects all error sequences with an odd number of bits.

Question 3 Show that the polynomial detects all error sequences of length 16 or less bits.

Question 4 Show that the polynomial detects 99.997% of all error sequences of length 17 bits.

Question 5 Show that the polynomial detects 00.998% of all error sequences of length 18 or more bits.

Problem 6.7: Anti-linear feedback shift registers.

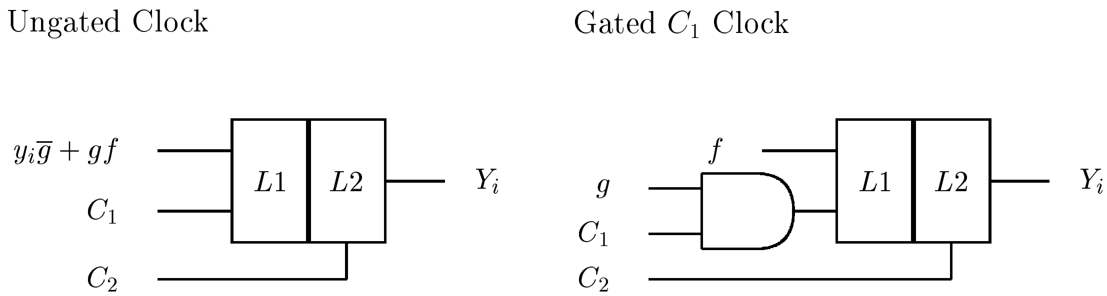


Two different linear feedback shift register implementations are shown in the figure. A simple modification to the LFSRs allows for the inclusion of the zero pattern into the sequence. Thus, using a LFSR of a primitive, characteristic polynomial, an exhaustive test pattern generator generating 2^n different patterns is created. The circuit is referred to as an anti-linear feedback shift register, ALFSR.

Question 1 Construct an External-XOR ALFSR.

Question 2 Construct an Internal-XOR ALFSR.

Problem 6.8: L1L2 design: Clock gating.



The figure shows two alternative implementations of the same function.

Question 1 Design a 2-bit binary counter using L1L2 latches.

Question 2 Show that the two circuits in the figure above both implement the function

$$Y_i = y_i\overline{g} + gf.$$

Question 3 Discuss whether or not the gated clock version is in accordance with the 6 requirements for LSSD design.

Question 4 Use the above realisation of the complex function to design a 3-bit binary counter.