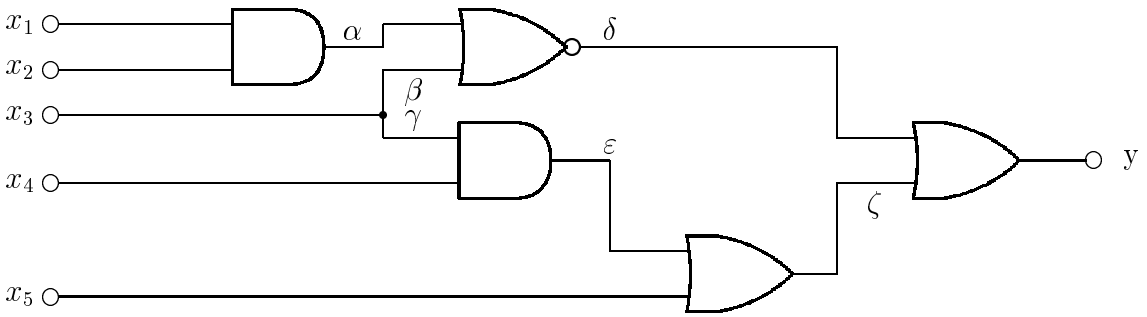
4 Test Pattern Evaluation

Problem 4.1: **Parallel fault simulation.**



Question 1 Consider the set of all single stuck faults in the circuit above, and perform fault collapsing.

Question 2 Arrange the collapsed set of single stuck faults in a 16 bit wide computer word. Simulate the test vector (0,0,1,0,0) and indicate detected faults.

Problem 4.2: **Deductive fault simulation.**

The circuit in Problem 4.1 is considered again for deductive fault simulation.

Question 1 Consider the two-input AND gate with inputs A and B and output Y. Determine the fault propagation rules under all possible combinations of inputs.

Question 2 Determine the fault propagation rules under all possible combinations of inputs for the two-input OR and NOR gates.

Question 3 The test vector (0,0,1,1,0) is applied to the circuit. Compute the fault lists and perform fault dropping.

Question 4 Second, the test vector (0,0,1,0,0) is applied. Perform event-driven evaluation and compute the updated fault lists.

Question 5 The third test vector (1,0,1,0,1) is applied. Perform event-driven evaluation and compute the updated fault lists.

Question 6 The fourth test vector (1,1,0,1,0) is applied. Perform event-driven evaluation and compute the updated fault lists.

Question 7 Next, the test vector (0,1,0,0,0) is applied. Perform event-driven evaluation and compute the updated fault lists.

Question 8 Finally, the test vector (1,0,0,0,0) is applied. Perform event-driven evaluation and compute the updated fault lists.

Problem 4.3: **Concurrent fault simulation.**

The circuit in Problem 4.1 is considered again for concurrent fault simulation. Only the collapsed set of single stuck faults are considered.

Question 1 Initially, the test vector (0,1,1,1,0) is applied to the circuit. Simulate the circuit and indicate the 'faulty gates' lists.

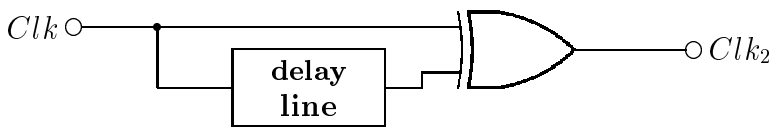
Question 2 Next, the test vector changes to (1,1,1,1,0). Resimulate the circuit and indicate the updated 'faulty gates' lists.

5 Testability Analysis

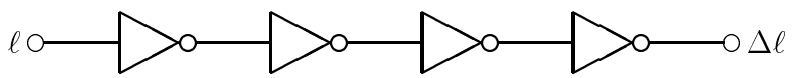
Problem 5.1: **Ad-hoc design rules.**

Discuss the testability of each of the circuit examples shown below.

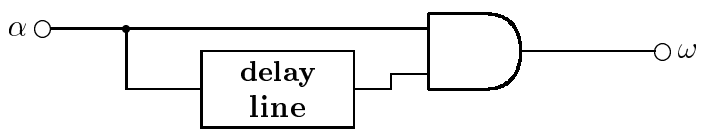
a. Double frequency clock generator



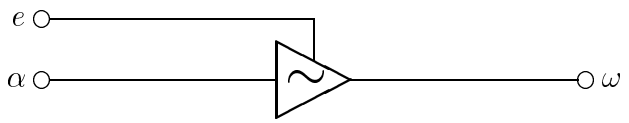
b. Delay line



c. Monostable

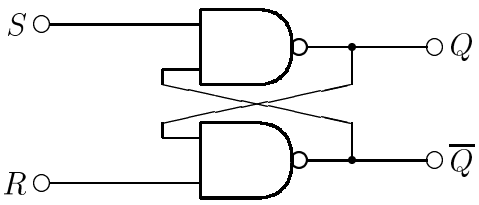


d. On-chip oscillator



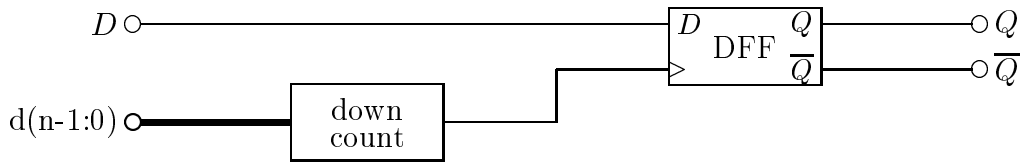
Problem 5.1: **continued.**

e. RS flip-flop

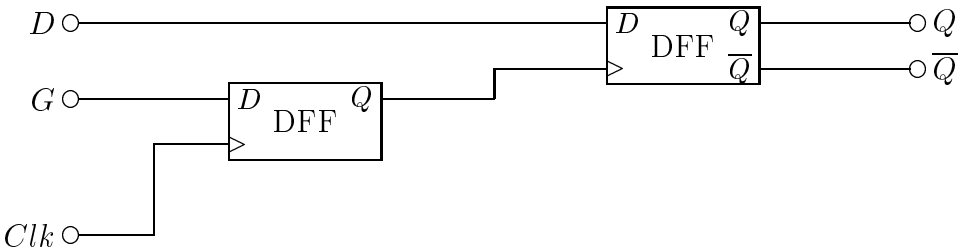


f. Implicit flip-flop

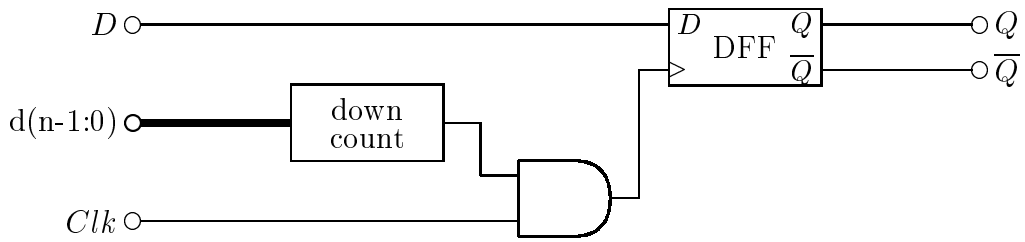
g. Decoder feeding clock input



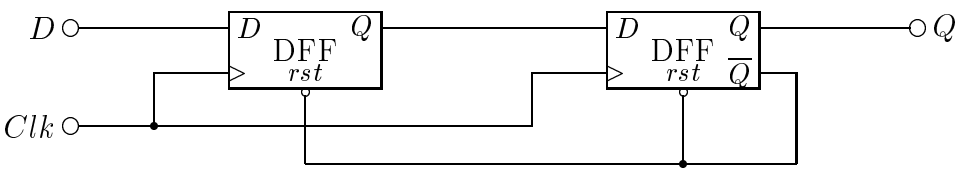
h. Latch feeding clock input



i. Clock gating

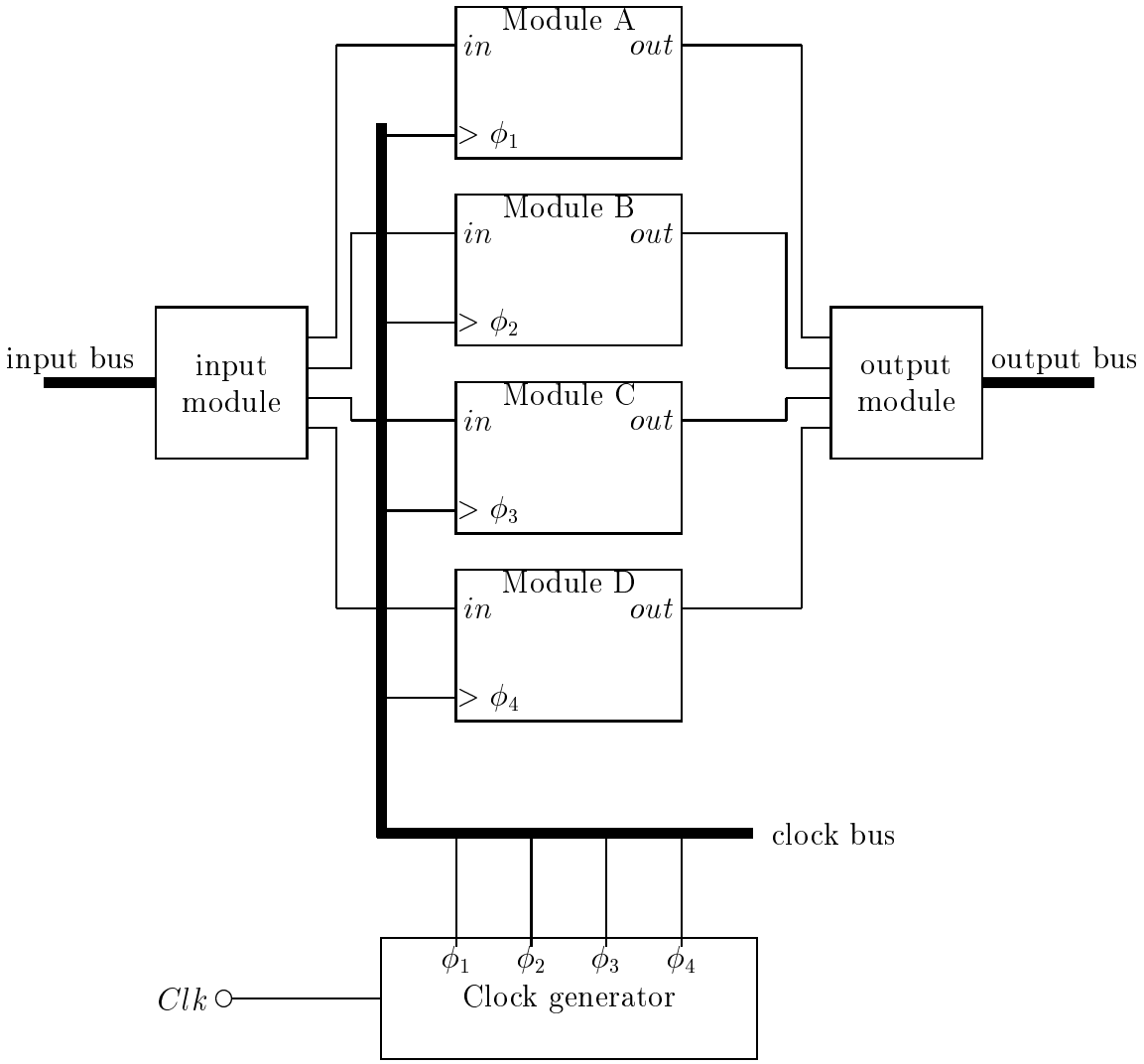


j. Asynchronously cleared DFF



Problem 5.1: **continued.**

k. Deferred clock generation



Problem 5.2: **COEDS Algebra.**

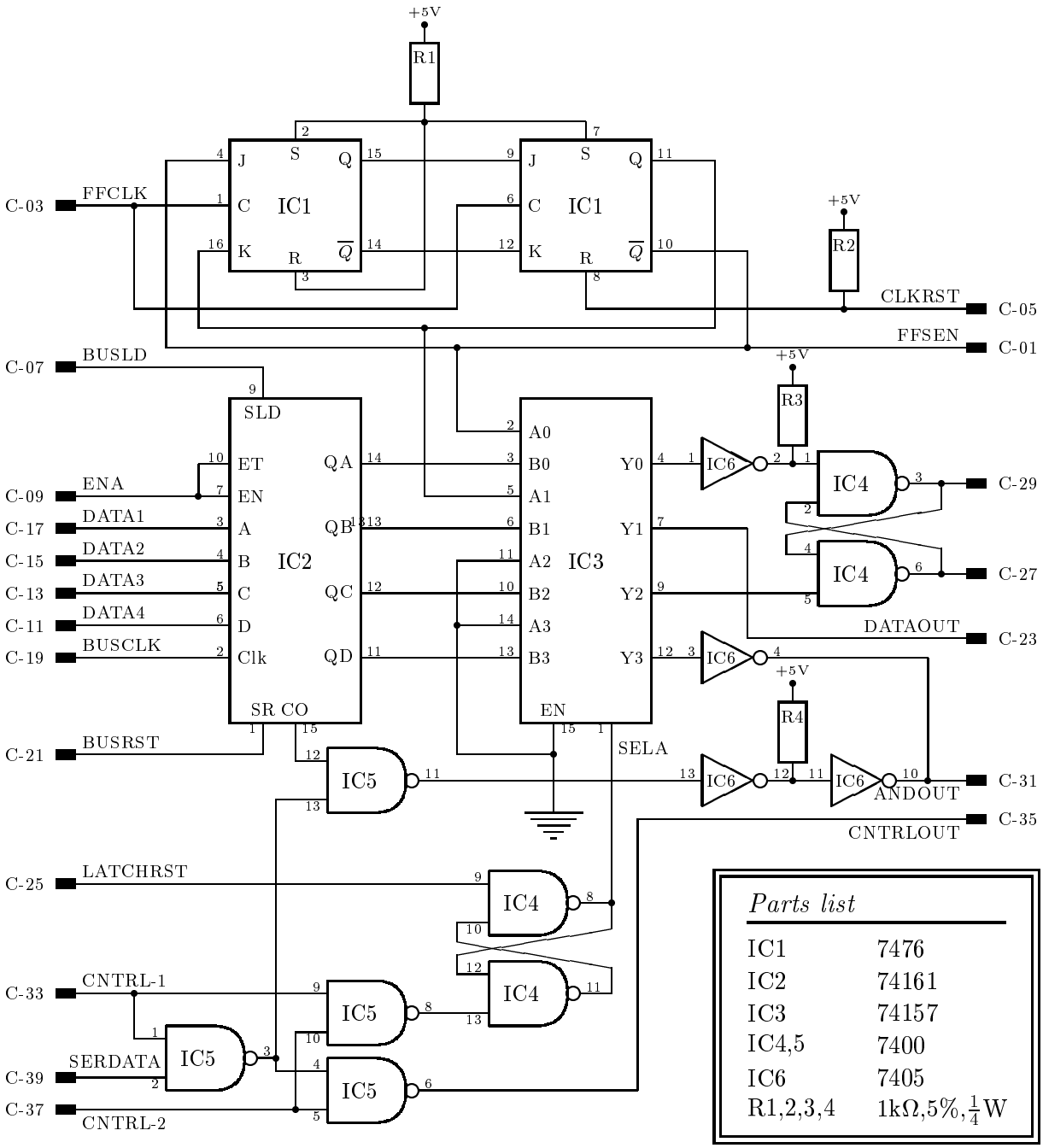
The COEDS macro model description language is used in this exercise.

Question 1 Construct the COEDS macro description for a 3-input EXOR (exclusive or) gate.

Question 2 Construct the COEDS macro description for both of the MOS transistors, nMOSt (n-channel device), and pMOSt (p-channel device).

Question 3 Discuss how the COEDS algorithm processes bi-directional devices such as MOS transistors.

Problem 5.3: **Design review.**



Parts list

IC1	7476
IC2	74161
IC3	74157
IC4,5	7400
IC6	7405
R1,2,3,4	1kΩ,5%,$\frac{1}{4}$W

Discuss whether the circuit in the figure is testable or not (Hint: Devise a test plan for the circuit).