Partial scan design using IEEE 1149.1 *

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Abstract

In this paper scan design is discussed. The methods of full scan, partial scan and boundary scan with IEEE 1149.1 (JTAG) are presented and explained. The various elements of JTAG are explained in detail. A patent from Motorola is presented to illustrate how to test devices with embedded memories for delay faults.

1. Introduction

Large VLSI devices are very hard to test if the tester only has access to the primary inputs and primary outputs. The test time for a complete test is dependent on the number of inputs and the number of states. Even a LSI device would normally be impossible to test within the expected lifetime of an IC.
So scan testing was developed to give access to the inner workings of an IC while minimizing the number of input/output pins added to the device for testing. This report will go through the AD-HOC methods of partitioning a design. The JTAG components will be presented and finally a method for at-speed testing of embedded memories will be presented.

2 Scan path testing.

Scan path testing, which is often refered to as scan test, is a technique for testing electronic circuits with a reduced requirement of I/O on the device. The disadvantage of the scan test is an increased in area because of the extra logic and this logic can also be faulty. The extra logic that performs the scan test decreases the speed of the IC.

In figure 1 is illustrated a model of a sequential logic network, which fundamentally covers a scan test and all such sequential logic network can be model as a network of combinational logic network and storage network. The secondary input and output are linking the logic network together with the storage network. The primary input may be controlled by some kind of state machine.

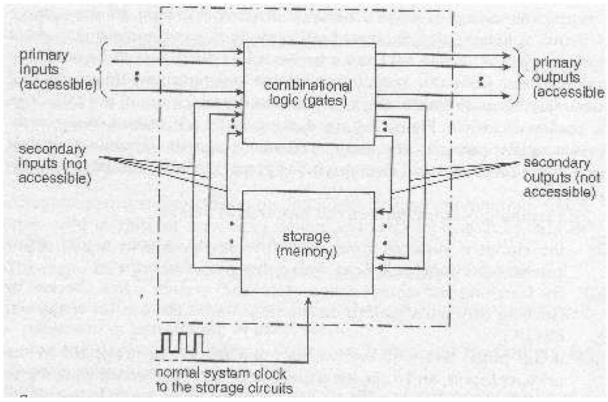

Figure 1. Scan-path testing of sequential network.

In order to control the behaviour of the scan path test, all the storage elements of the circuit are switched form a normal mode into a test mode by shifting register input values. Figure 2 illustrates scan test, where scan-in I/O and scan-out I/O can read and write the value of storage element.

Switching from normal mode to test mode is done by using multiplexer to control whether the register should load the secondary output of the combinational logic network or the scan-in input as shown in figure 3. The output of the register is either loaded as secondary input or serially as scan-out.

3 Introduction to Partial Scan Path

Scan path testing is a means of adding controllability and observability to a sequential circuit. This is achieved by adding and/or reconfiguring existing storage elements (latches, flip-flops), and then running the circuit in either

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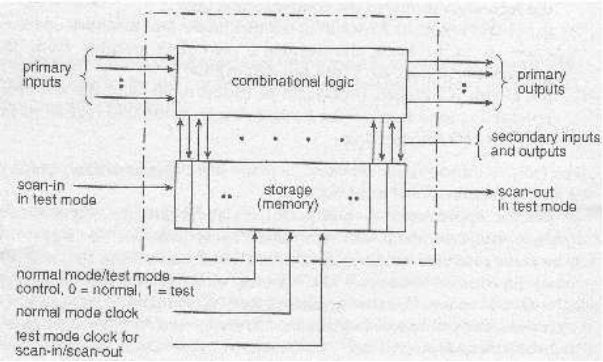

Figure 2. A shift register scan-in/scan-out of a storage element in test mode.

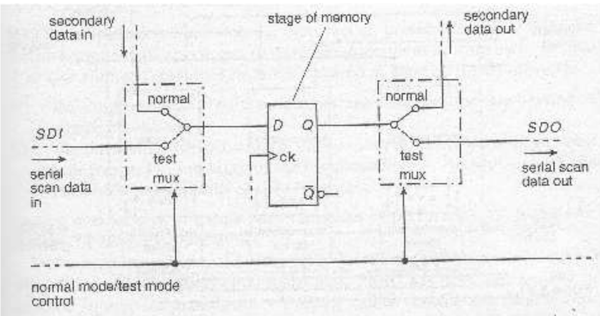

Figure 3. The multiplexing requirements on each stage of the storange network.

normal or test mode. Different guide lines on how to partition a circuit and which storage elements is to be included in a scan path has been proposed for partial scan designs.

3.1 Full Scan Design Drawbacks

- Since full-scan testing requires sequential test patterns and combinational circuits require very few secondary inputs, the registers and combinational therefore cannot be tested separately.
- States of stages remain unaltered after a number of test vectors, and secondary inputs will carry faults into a small number of memory elements *test vectors could be shorter*(only a few number of storage elements are interesting)

All the above drawbacks of full scan testing lead to the implementation of partial scan design, which in general minimizes the size of test vectors needed to be scanned in/out, and not to introduce any new I/O pin requirements.

3.2 Partial Scan Path Partioning Methods

When partitioning the circuit, some crucial points need to be held:

1. In order to decrease or keep present testing and normal execution time, components added to the circuit need to be held at a minumum.
2. Registers added to the circuit for testing purposes need to be kept out of the critical path so as to ensure the normal execution speed does not increase.
3. Signals added to the registers used for scan in/out need to be kept at a minumum so both testing and normal execution modes are not increased due to adding extra signals.

3.2.1 I-Paths

One form of partial scan [3] introduces the concepts of I-Modes and I-Paths, which have the purpose of:

1. Identifying a subset of registers to be included in the scan path.
2. Scheduling the testing of logic blocks since it is not always possible to test all blocks simultaneously.
3. Determining efficent ways to activate the control lines when testing a block of logic.
4. Determining ways of organizing the scan paths to minimize the time required to test the logic.

The article [3] or text book [2] do not go much in details with these concepts, but the article dos give a circuit example.

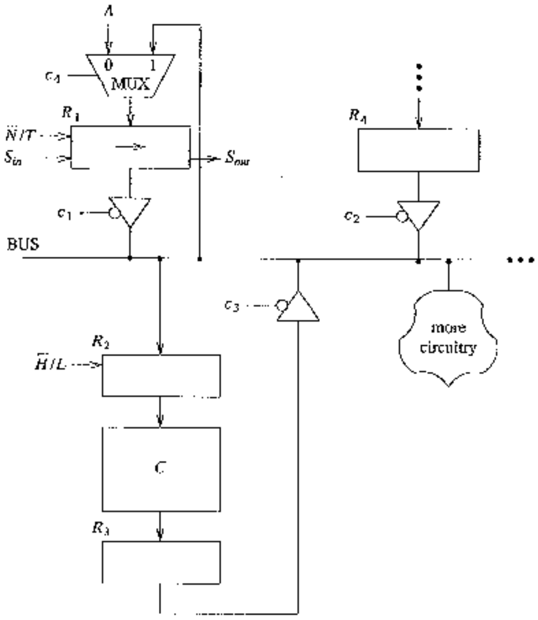

Figure 4. I-path testing

First I-Paths are identified (data is not altered throughout the path) in order to find a set of registers to be included. A test register is then identified to be able to test x number of combinational circuits. From the set of registers is also chosen ones to hold/capture the input/output from the tested combinational circuits. From the in figure 4, the I-Paths exists from the output of the combinational block C to the inputs of R1, R2, R3 and from the outputs of R1, R2, R3 and R4 to the input of C.

3.2.2 BALLAST (Balanced Structure Scan Test)

The BALLAST [4] methodology sets out certain guide lines for the selection of storage elements which shall be reconfigurable and make sure that the unaltered storage elements are in an acyclic configuration. This method is said to need combinational ATG computation only even though the circuit is sequential.

The combinational logic can be partitioned into so called maximal regions referred to as clouds. The inputs to a cloud are either primary inputs or outputs from a storage element. The outputs from a cloud is either primary outputs or inputs to a storage element. A group of wires forms a vacuous cloud if it:

1. Connects to the outputs of one register directly to the inputs of another register.
2. Represents primary inputs feeding a register.
3. Represents the outputs of a register that are primary outputs.

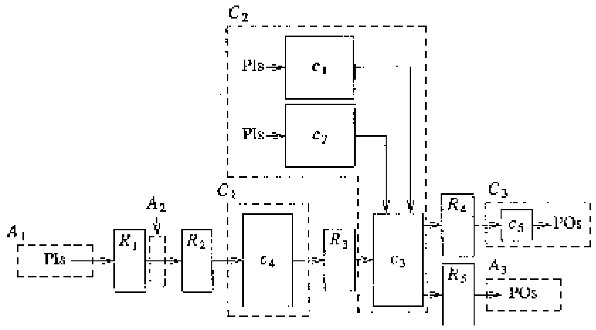

Figure 5. BALLAST circuit clouds

From the figure 5 A1, A2 and A3 are vacuous. A1 and A3 apply to item 2 and 3, where A2 applies to item 1. The combinational portions of the circuit are not vacuous. Because there are an equal number registers on all signals between two vacuous clouds, the circuit is considered *balanced*. On the other hand, if there had been a register introduced on the output after c_5, then the circuit would have been *un-balanced*.

According to [2], BALLAST says the ideal grouping of storage elements are found by:

1. Each group of storage elements must have the same clock and control lines to all storage elements (this is usually the case and is nothing extraordinary).
2. Each group must have secondary input data from only one partition of the combinational logic.
3. each group must feed secondary output data to only one partition of the combinational logic.
4. There shall be no cyclic sequential actions within the groups which are not reconfigured into scan-test configurations, that is the non-reconfigurable group shall be acyclic.
5. All paths between two combinational logic partitions separated by non-reconfigurable groups of storage elements shall have the same number of clocked storage elements in series such that the signal delay ia all paths is the same (termed balanced)

The above conditions ensures that there are no cyclic(sequential) action to be handled by the test pattern generation i.e. *no sequential test patterns to be generated,* *making it less complex for testing and test pattern generation*. It is important first to create the clouds and then cluster storage elements, else it is possible that only one cloud can be identified. For some circuits, however, acyclic balanced structures may not be feasible due to physical or economical constraints.

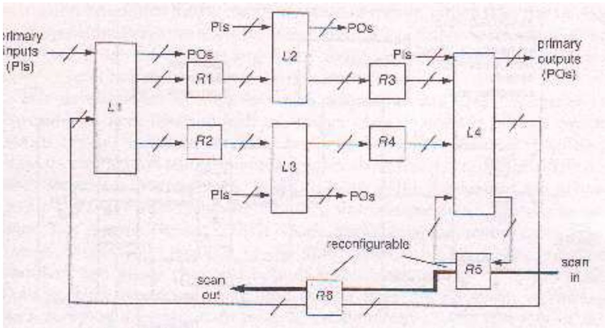

Figure 6. Paritioning BALLAST circuits

The procedure for scan test of the circuit figure 6 is as follows:

1. Scan in appropriate test bits into R5 and R6, which in scan mode, become primary inputs and outputs, respectively.
2. Load the test bits from R5 and R6 into L4 and L1 and apply the remaining test data to the primary inputs.
3. Keeping all these test bits unchanged , clock the non-reconfigurable storage elements R1, R2, R3, R4 an appropriate number of times to transfer resulting data from L1 to L2 and L3 and on to L4. Because the non-reconfigurable storage elements are acyclic a steady-state condition will be reached throughout the circuit L1 to L4.
4. Check the test response on all primary outputs.
5. Scan out and check the secondary outputs from L4.
6. Repeat using the next test vector.

Other scan designs could have been used and the circuit in question should be investigated to find a superior design. Finding a design with the fewest number of storage elements in the scan path or finding a design which is less sensitive to the delay introduced by making registers in to scan registers.

3.3 Testing Partial Scan Path Partitions

This part describes three guidelines for partial scan path partition testing. Partial scan has been proposed to provide a faster test procedure then for full scan, by choosing a subset of registers to be included in the scan path. Speed performance is gained because less reconfigurable registers(scan registers) are used, which introduces delay into the circuit due to increased complexety, since less are used less delay is added to the circuit. For the same reason partial scan designs have the advantage of redusing the circuit overhead

3.3.1 Multiple Test Session

Partitioning a circuit into smaller blocks it is possible gain some advantages in terms of test speed and complexity. This type of partitional testing can be accomplished in several ways. can be done in three modes:

- *together mode*
- *separate mode*
- *overlapped mode*

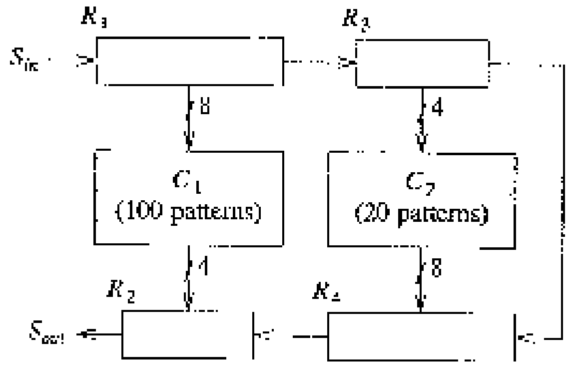

Figure 7. Testing using multiple test sessions

In *together mode*, test vectors are appended together then shifted into the input registers. The outputs are read into the output registers simultaneously, then read out serially. The different number of test vectors for combinational blocks, however, could be considered wasteful, since many *don't cares* are in the remaining test vectors.

In figure 7, the combinational blocks C1 and C2 are tested together, where C1 has 8 inputs and 4 outputs and can be tested using 100 test patterns and C2 has 4 inputs and 8 outputs and can be tested using 20 test patterns. This means that the entire circuit can be tested using 100 test patterns of each 12 bits (input to C1 is 8 bits + input to C2 is 4 bits = 12 bits) this results in a total test time of 100*12 = 1200 clock cycles not including the time it takes to scan in the test vectors in R1 and R3 and the time to scan the results out of R2 and R4.

In *separate mode*, while one circuit is being tested, the other is being ignored along with the other's input and output registers. Based on the given combinational circuits, the appropriate bit lengths are fed into the primary inputs of the circuits, and the outputs are read serially out of the output registers, where each circuit is tested separately.

In figure 7 C2, R3 and R4 would be ignored while testing C1 and only R1 would be loaded. Since the max bit length of the data entering and leaving C1 is 8 only 8*100 = 800 clock cycles is to test C1. To test C2 the scan path need to be reconfigured by having the scan output of R4 drive a primary output. This can be done by disabling the loading of data from C1 to R2. Then C2 can be tested by loading the 8 bit(4 bit input to C2 + 4 don't care bits) test vectors into the scan path formed by R1 and R3. This gives 20*8 = 160 clock cycles to test C2 and a total time of 960 clock cycles to test C1 and C2 which is less then the previous case where 1200 clock cycles was required.

In *overlapped mode*, the combinational circuits are tested together for an appropriate number of common test vectors. Following the completion of the initial test vectors, the combinational block lacking test vectors is then put into separate-mode and tested with the remaining test vectors.

In figure 7 C1 and C2 are initial tested together with 20 test patterns of 12 bits = 240 clock cycles, then the test of C1 is completed by applying the remaining 80 test patterns of 8 bits = 640 clock cycles, thus giving a total of 880 clock cycles to test the circuit

4 Partial Scan Testing Elaboration

Partial scan testing presents a method for limiting hardware overhead and the execution time. The basic functionality of the methods are as follows

- Identify storage elements of the circuit.
- Choose storage elements to be include in the scan path, in order to maximize fault coverage and minimize the length of the test sequence.
- Avoid placing registers on critical path to ensure normal execution speed.
- Partition circuit according to locations of the chosen scan path storage elements and the associated combinational parts.
- Use ATG program to generate minumum number of test vectors for each combinational part, and try to minimize length of vectors
- Determine test scheduling scheme to use, then test.

Unfortunately, it increases the complexity testing by demanding more housekeeping of control signals and test vectors and responses.

5 Boundary scan and IEEE standard 1149.1

Boundary scan is concerned with delivering a signal and receiving a signal for I/O in a sequential logic network. Testing is normally done on an individual unconnected IC.

The Joint Europe Test Action Group (JETAG) was established in 1985 by developers of boundary scan and was later called JTAG, when developers from North America joined them. The work of the JTAG organization resulted in the IEEE Standard 1149.1-1990, entitled the standard test access port and boundary scan architecture.

The idea of a boundary scan is to place a boundary scan cell in every I/O pin of a circuit. This is illustrated in figure 8. Figure 9 illustrate a boundary scan cell.

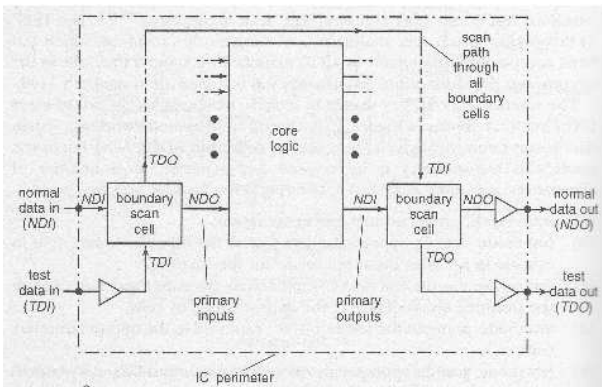

Figure 8. Provision of a boundary scan cell on every I/O of an IC

The test data in corresponds to TDI and test data out corresponds to TDO. The signal TMS is used to control the behaviour of the boundary scan cell and TCK is used for clock of the register.

It is possible to make boundaries on multiple ICs on a test board with the four signals: TDI, TDO, TMS and TCK, all of which are shown in figure 10.

Using the protocol in this manner to test the IC is called the JTAG four-wire test bus. The figure also show that to test an IC, a test access port (TAP) controller is also required, which receives and sends the four signals. The design of the TAP controller and the boundary scan cell may vary between IC vendors, but they all have to obey the protocol laid in the specification of 1149.1. The behaviour of

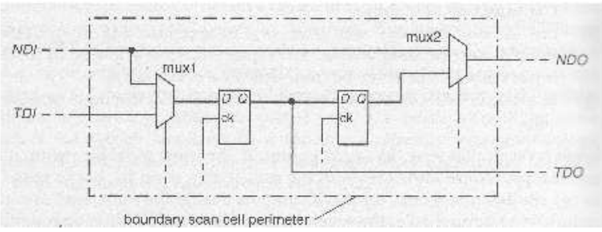

Figure 9. Simplified details of one boundary cell circuit, omitting clock and control signal

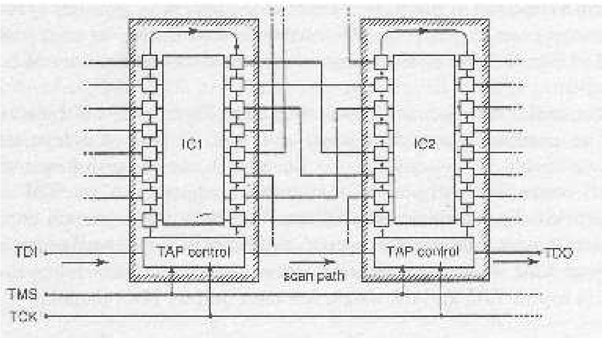

Figure 10. A scan path through a number of ICs in series

the TAP is determined by the TMS and TCK. The TAP controller is an 16 state Moore finite-state machine which is shown in figure 11.

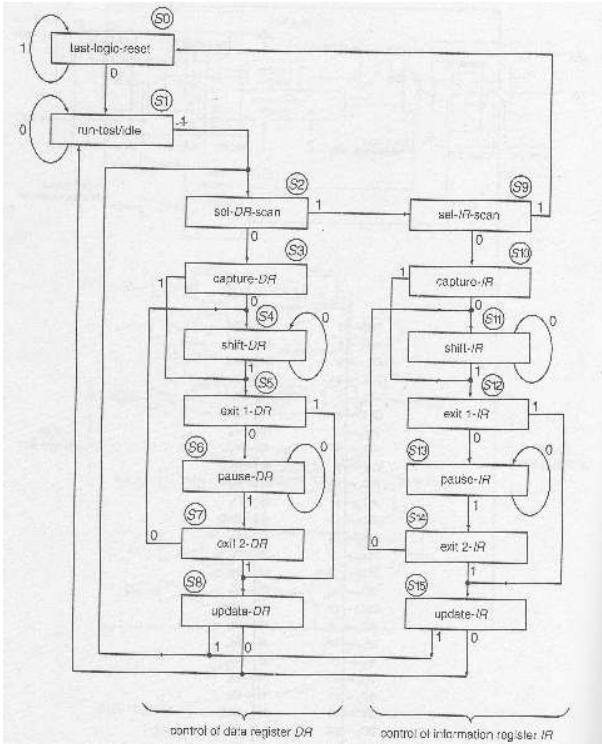

Figure 11. The state diagram for a TAP controller. The value of TMS required for each state transition shown on the link between state, all transitions being on the rising edge of clock TCK

It is possible to combine partial scan design with IEEE 1149.1 boundary scan design. It only requires that the JTAG four-wire test bus as protocol to control the behaviour of the IC. This is done by replacing the multiplexer, which is used to shift the stage of the storage network (Figure 3), with the TAP controller and the boundary scan cell.

6 Scan design techniques for delay testing

There are two typical delay tests that are invoked on a design and that is delay path testing and delay testing. Delay path testing tests externally for the delay as presented by team 1 earlier in the course. Delay testing means testing and verifying the correct functionality of the critical paths in an embedded design. The critical paths usually involve large blocks that are difficult to control, e.g. memory elements. Delay testing is the focus of this section of the report.

Delay testing with scan paths means testing a system at-speed to verify that no fabrication errors exist that gives a increase in the delay of a certain path that causes errors in other paths that depend on the path with the error.

Problems arise when having to test an IC with embedded memory. For testing, the output of the memory must be controllable, therefore many test strategies consist of bypassing the memory with a controllable signal. This causes the fake memory-data to be present much faster than when using the actual memory. So it is not possible to test the memory at-speed. However, a patented method from Motorola solves this problem.

6.1 BIST

The embedded memory itself is tested for stuck-at faults with MemBIST[1]. Embedded memory is usually a component in a repository of black-boxes in a company or maybe an IP core from a 3rd party vendor. So testing should already be a part of that component.

6.2 The patent

In 1997 Motorola patented a method for ”Scan based path delay testing of integrated circuits containing embedded memory elements” (See [1]) . The patent describes how to test combinatorical logic and embedded memory at-speed while still controlling the output from the memory. The invention is motivated by the fact that Automatic Test Pattern Generation (ATPG) tools can’t generate tests that cover embedded memories.

The patent first explains the basic concepts of testing and discusses the problems with testing embedded memories. The problem is that the circuit suddenly doesn’t have a simple homing sequence since the memory isn’t a state machine. This means that ATPG tools basically give up.

The maximum speed of an IC is determined by the slowest path through the device. This path is called the ”speed path” . Such a path is usually dependent on the embedded memory since memory access is very slow compared to combinatorical logic. The problem is seen in figure 12 (figure 2 in the patent) where path A-B-C is the slowest. The scanable registers before and after the memory enables scan testing. The scan registers can run at the same speed as the combinatorical elements but the embedded memory might run at a separate (faster) clock so at-speed testing is not possible.

[1]Memory Built-in-self-test

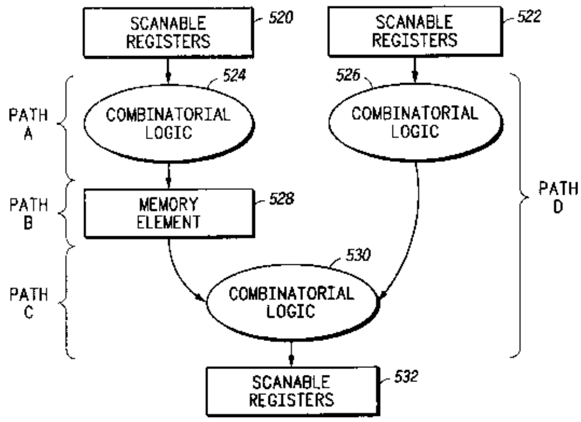

Figure 12. A design with embedded memory

6.3 First proposed setup

The first setup proposed is seen in figure 13 (Figure 4 in the patent). The functionality of the circuit is controlled by the signal SCAN MODE (570). When this signal is 0, the requested memory element is fetched normally. First the address is decoded (572) and the row address is sent to the memory array (583).
When the design is in SCAN MODE, the row address decode is bypassed and only the dummy decode is used. The row driver (578) then tells the memory cells to fetch the dummy row. The sense amps checks that the memory has fetched the dummy row and then outputs the WRITE DATA IN (564) signal. In this mode of operation the memory is only a delay function. A simplified figure illustrating this is 14 (Figure 7 in the patent).

6.4 Setup with separate dummy logic

Another setup of the invention is shown in figure 15 (Figure 5 in the patent). This setup allows the memory to be completely detached from the rest of the logic because the dummy decode (574) and the dummy row (581) are separated from the actual embedded memory (582). With this setup the memory can perform BIST while the combinatorical logic is tested simultaneously. This is called burn-in mode.
For this setup a clock is needed to run either scan mode or burn-in mode.

6.5 Controllable memory output

The third setup in figure 16 (Figure 6 in the patent) is very similar to the first version but the dummy row (581) is not controllable by the write data drivers (580) and hence the output from the ”memory” is controllable in scan mode.

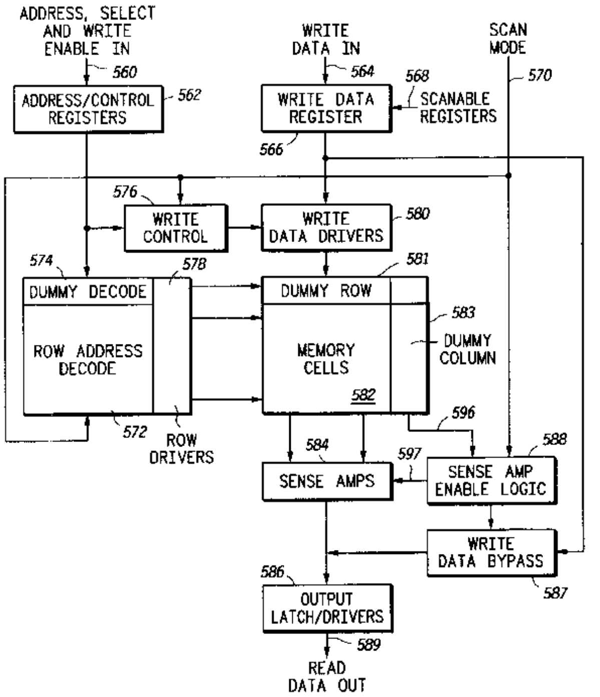

Figure 13. The first proposed setup

This allows the test to involve data read from the memory.

6.6 Sense amp enable logic

The patent gives a diagram of the sense amp enable logic that is the core logic around the invention. The circuit has 3 inputs that are asserted by the tester: READ (598), TIMING SIGNAL (596) and BYPASS (599). The circuit is shown in figure 17 (Figure 8 in the patent). The read and bypass signals are used to either detect the memory output (read mode) or select the write data in signal (bypass mode). The

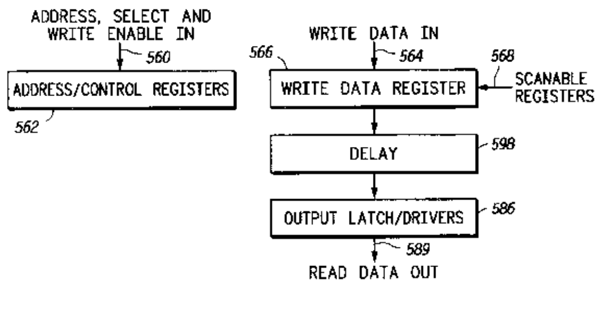

Figure 14. The memory functions as a delay function in scan mode

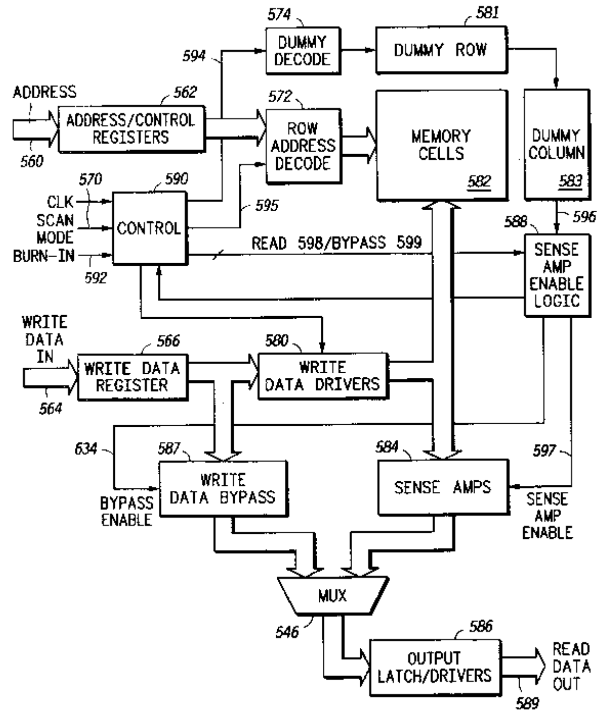

Figure 15. The second setup with burn-in mode

timing signal works as a clock.

6.7 Control block design

The final figure in the patent is the control block. This is the block that enables burn-in mode that allows the memory to run BIST. The logic is pretty simple as seen in figure 18 (Figure 9 in the patent). It selects whether to read the memory, bypass the memory and/or completely cut off the memory. The control block is a part of the setup in figure 15.

6.8 Conclusion on the patent

The patent solves a very difficult problem, i.e. testing embedded memory in a simple manner without adding excessive logic. Scan testing already adds some extra area to the design so a manufacturer will be interested in adding new test methods without adding even more area.

References

[1] R. Y. D.M. McCarthy, P.W. Hollis and R. Eisele. Scan based path delay testing of integrated circuits containing embedded memory elements. *US Patent 5,761,215*, June 2 1998.

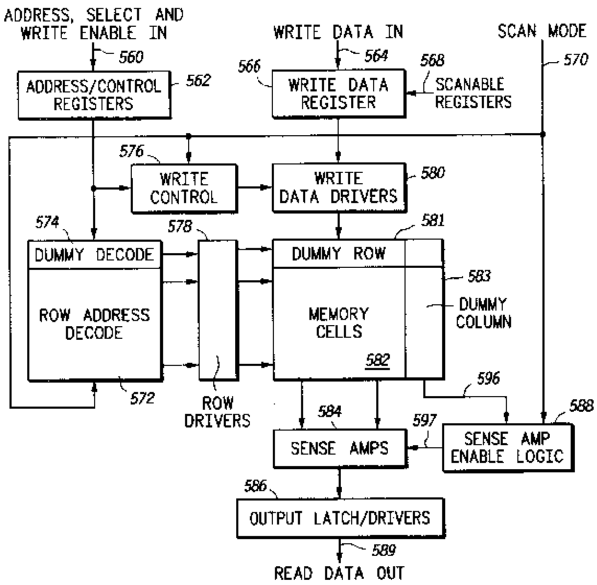

Figure 16. The first setup with controllable memory output

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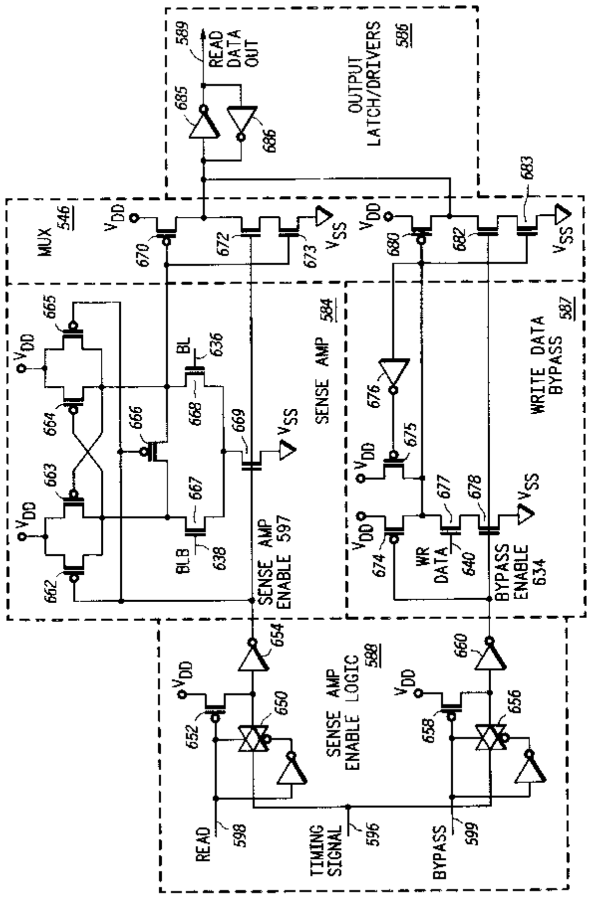

Figure 17. The sense amp enable logic diagram

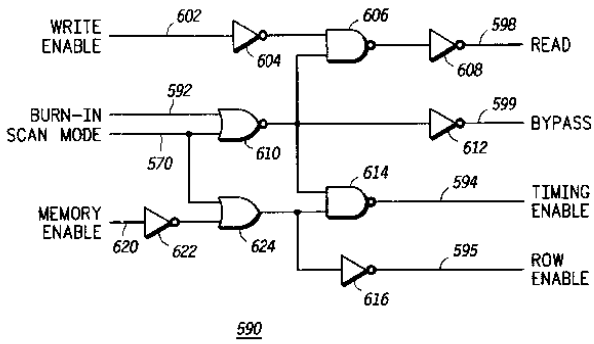

Figure 18. The control block