Partial Scan Design Using IEEE 1149.1 *

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Abstract

Scan design technique is a well known method of design for testability in which designer chains all flip-flops in the circuit into one or more shift registers.All the circuit registers can be controlled and observed for the primary input and outputs .It becomes easy to partition the sequential circuit into a combinational one that can be tested.In full scan design all flip-flops are included in the scan register ,which costs area overhead.In partial scan we can optimize the area by using selected number of flip-flops and excluding the flip-flops on critical paths to avoid the un acceptable timing penalties.In this paper we discussed different issues related with design of partial scan and delay testing in perspective of IEEE 1149.1.

1. Introduction

Scan design methodology as a design for testability has become a popular technique for sequential circuits.In scan design test mode control signals are added to the circuit and flip-flops are chained together to form a shift register in order to make the primary input and output of shift registers to be controllable and observable[1].In a full scan design all flip-flops are chained together into one or more shift registers to observe and control the internal states from primary input and output.To test a sequential circuit we can divide it into combinatioanl and shift register parts.The cost of Test pattern generation will be substantially low because automatic test generation programs are available for combinational circuits.

On the other hand Partial scan techniques have been widely accepted as an effective solution to improve sequential Automatic Test Pattern Generation performance while keeping acceptable area and performance overheads.Several techniques for flip-flop selection based on structural analysis have been presented in different papers and literaure.

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Because all flip-flops are not included in the scan register therefore arae overhead is lower and we can minimize unacceptable timing penalities by excluding the flip-flops on critical paths.Critical paths and their timing margins are easily determined with automatic tools.In partial scan we can optimize the area and minimize the timing but at the same time we loose fault coverage.In full scan flip flop faults are covered by shift register tests while in partial scan the faults in unscanned flip-flops cannot be tested.

In section 2 of this report we will discuss the boundary scan technique according to the IEEE standard 1149.1,in section 3 and 4 we will discuss the issues realted with partial scan daseign and delay tetsting.

2. Partial and Boundary scan-using IEEE 1149.1

Historically most most PCB testing was done using bed of nail test equipments,but due to the marginal increase in circuit density and new techniques in fabrication make it almost impossible to check in-circuit functionality with previous techniques.Considering it as an emergent requirement a group of European Companies formed Joint European Test Action group(JETAG) to tackle these challenges.It called for incorporating hardware into standard components which is to be controlled via software to eliminate for sophisticated in circuit test equipment. In 1988 in North America several other companies formed the Joint test Access Group(JTAG).In 1990 IEEE refined the concept and created 1149.1 standard,known as IEEE standard Test Access Port and boundary scan architecture.At the moment the valid standard is IEEE 1149.1 -b.

The advantages of Boundary Scan technique are as follows [2].

. No need for complex test equipments for testing PCB's

. Less time for test pattern generation and application

. Higher fault coverage

. Reduced work for test engineer

2.1. Description Of Boundary Scan

Boundary scan is a methodology allowing complete observability and testability of boundary pins of a JTAG compatible device via software control.Following figure[1] illustrates possible structures for input and output pins of a JTAG compliant device .

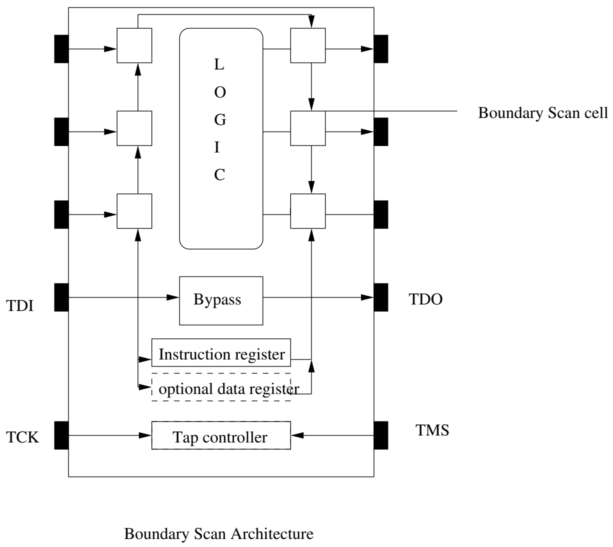

Figure 1. Boundary scan Architecture

During standard operation boundary cells are inactive and allows data to be propagated normally through the device .The operation of these scan cells is controlled through the Test Access Port controller and Instruction register. The block diagram of TAP controller is mentioned in figure [2] and state diagram of controller is mentioned in figure[3]

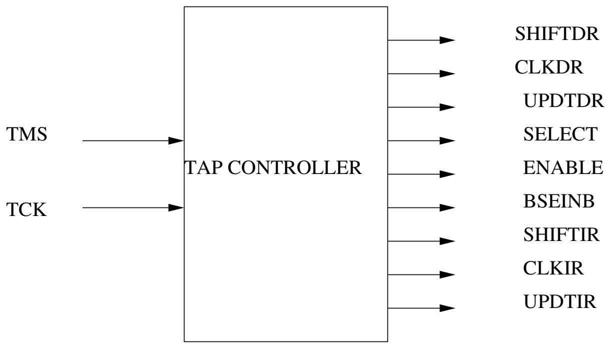

Figure 2. TAP controller block diagram

The Test Access Port controller is a Finite State Machine with 16 possible states which control operations associated with boundary scan cells.The basic operation is controlled through four pins

. Test Clock(TCK)

. Test Mode Select(TMS)

. Test Data In(TDI)

. Test Data Out(TDO)

Test clock (TCK)and Test Mode Select(TMS) pins direct signals between TAP controller states.There is an optional pin TRST can be implemented as an asynchronous reset signal to the TAP controller.

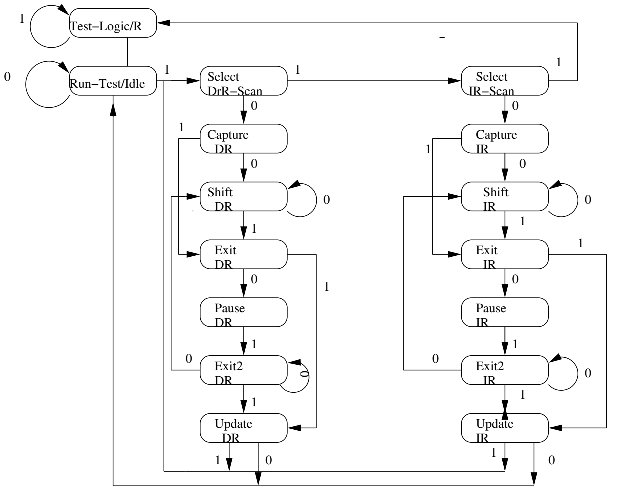

Figure 3. State diagram of TAP controller

Following registers are required in IEEE 1149.1 standard

1.Instruction register:

The instruction register is responsible for providing the address and control signals required to access a particular data register in the scan path . The Instruction register consists of three IR cells.Each cell has a shift register stage and a latch stage.On capture state the shift register is loaded which is used for fault isolation of the board level serial test data path.Data in the shift register is shifted toward TDO,and data in the latch remains the same. The data in the shift registers is latched out and becomes the current instruction on the falling edge of the TCK in the update IR state.During the Reset state it corresponds to the BYPASS instruction.

2.Data Registers:

Two data registers are required one is boundary-scan register and other is BYPASS register, with a third, optional device identification register.Data registers are arranged in parallel from the primary TDI input to the primary TDO output.During the scan operation the instruction register supplies the address that allows one of the data registers to be accessed.During the register scan operation the addressed scan register receives TAP control via the data register shift enable and data register clock inputs to preload test rresponse and shift data from TDI to TDO.

2.1Boundary-Scan Register:

The boundary-scan register consists of a series of boundary-scan cells arranged to form a scan path around the boundary of the host IC.The Boundary scan cells provide the controllability and observabilityfeatures required to perform boundary scan testing.

2.2 Bypass Register:

The bypass register consists of a single scan register bit.After selecting the bypass register,it provides a single-bit scan path between TDI and TDO.The bypass register is selected when instruction register is loaded with a pattern of all ones.

2.3 Chip Identification Register:

The chip identification register is an optional register to identify the specific information.

There are total nine test instructions in which three are required , rest are optional.Three required test instructions are mentioned below

. BYPASS Instruction

The BYPASS instruction allows the chip to remain in a functional mode and selects the bypass register to be connected between TDI and TDO

. SAMPLE/PRELOAD Instruction

This instruction also allows the chip to remain in its functional mode and select the boundary scan register to be connected between TDI and TDO.

. EXTEST Instruction

The EXTEST instruction places the chip into an external boundary test mode and selects the boundary scan register to be connected in between TDI and TDO

The rest of six instructions are optiional and could be use according to the requirement.

3. Testability complications of sequential circuits

In recent years, DFT techniques employing scan design methodology have emerged as the standard for testing of complex VLSI chips. The scan designs, when carefully planned and implemented, can give a significantly high fault coverage at reduced effort time and cost, invested in ATPG equipment for complex synchronous designs. Many sequential circuit test generators have been devised on the basis of fundamental combinational algorithms. As shown in Figure 1, a combinational model for a sequential circuit is constructed by regenerating the feedback signals from previous-time copies of the circuit. A time-frame, represents a copy of the combinational portion of the circuit. The inputs of a time-frame include the primary inputs (PIi , i = 1, . . . , n), and the outputs of the flip-flops, called the present state lines (PSi , i = 1, . . . , m). The outputs of a time-frame include the primary outputs (Oi , i = 1, . . . , k), and the data inputs of the flip-flops, called the next state lines (NSi , i = 1, . . . , m). A clock pulse needs to be applied between two time-frames to update the values at the present state lines of one time-frame from the next state lines of its previous time-frame. This combinational model is used to approximate the timing behavior of the circuit. Due to time frame unfolding, a single fault in original sequential circuit is represented by multiple fault in the iterative logic array model.

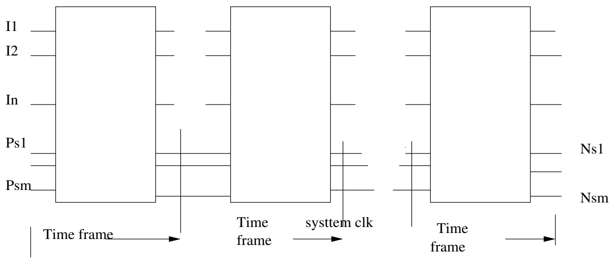

Figure 4. conventional iterative-array model of a sequential circuit

The Automatic Test Pattern Generation (ATPG) for testing of sequential circuits is the most challenging task in electronic design automation. The root cause of this complexity lies in the poor controllability and observability of sequential components, memory elements and cyclic nature of most of sequential circuit designs. The ATPG process for a given fault consists of three phases: fault initialization, fault activation and fault propagation. Fault initialization specifies the signal values for fault activation for a given fault model. In fault propagation phase, effects of fault are propagated to PO. It consists of two inter-related processes of justification and implication of fault values. Justification requires decision making and the new values assigned during justification process can uniquely determine the values on some other signals. As the operation of sequential circuit is modeled by iterative array model, fault initialization and activation requires multiple clock cycles. The circuit may have to go through several time frames before its response can be observed at PO. Similarly, after the fault is activated, it may not be possible to propagate its effects to PO in same time frame, i.e., it may as well take several clock cycles. Handling highly sequential circuits can be extremely hard due to large number of time frames required. For example, only in the fault initialization phase of testing process, activation of a stuck-at-0 fault at most significant bit of a 32-bit sequential counter requires 2**32 test patterns . Therefore sequential ATPG is by no means a complete solution for highly sequential circuit. Unlike the combinational circuits, sequential circuits require test vector sequences instead of single input vector. It is extremely hard for ATPG equipment to cope with such large requirement of test sequence generation. Most sequential circuit test generation approaches neglect circuit delays during test generation. Such approaches primarily target synchronous or almost synchronous sequential circuits and cannot properly handle highly asynchronous circuits whose functions are strongly related to the circuit delays and are sensitive to races and hazards. Moreover, due to the memory elements, sequential circuits have poor observability and controllability as compared to the combinational circuits. The next-state outputs from the combinations part of a sequential design are fed to the flip-flops, whose output is fed again to combinational circuit on subsequent clock cycle. Due to this closed feedback path through the flip flops, it is not possible to control or observe the flip-flop inputs and outputs under ordinary circumstances, except for those which have their inputs and outputs directly connected with primary inputs(PI's) and primary outputs (PO's). As the number of flip-flops are dramatically increasing, any scheme that can reduce the complexity of automatic test generation process is very attractive.

3.1. Scan based design for VLSI testability

In light of above mentioned reasons, sequential ATPG is by no means a complete solution for testing of sequential circuit. Sequential ATPG combined with an appropriate DFT technique, such as scan designs, are very attractive test alternatives.

In Full scan approach, each flip-flop is preceded by a multiplexor, which can choose between either the next state variable input or the scan in input, depending of the applied mode control input. These flip-flops are chained together to form the scan register. Thus in the scan mode, test vectors can be scanned in the scan register and the circuit response to this test vector can be observed at the scan out output, overlapping in time with shifting in of next test vector in the scan register. This not only enhances the controllability and observability of sequential components of circuit under test but also makes it possible to make use of the ATPG equipment for combinational circuits with slight modification.

Although full scan designs offer a high degree of testing reliability and fault coverage, those do not come for free. Scan designs have a considerable overhead in terms of area, power consumption and performance degradation. The latter comes from addition of multiplexors, which may lie in the critical path of the circuit, and very long scan registers in case of a complex design. According to [2], extra hardware overhead can be about 30

Extensive research in the area of the sequential circuit testing reveals that all the flip-flops do not required to be scanned and almost same results can be achieved by selective flip-flops in sense of fault coverage. This highlights the basic philosophy of the partial scan designs for the sequential circuits. Significantly lesser number of flip-flops can be chosen for scanning which avoid the area and additional hardware overheads involved in the case of full scan design. The selection process of flip-flops is guided by different heuristics which take into account different properties and factors to ensure the close to optimal performance of testability design. The decrease in the fault coverage when using partial scan design arises from the fact that the I/O of the flip-flops that are not included in the scan chain cannot be controlled or observed. Therefore some of the faults that are present in these flip-flops cannot be detected. It is proved [6], that using the partial scan process simplifies the task of automatic test generation. If the circuit can be represented by acyclic S-graph, the combinational ATPG can be used with slight modification.

3.2. Flip-Flop Selection for Partial Scan Designs

Scan flip-flop selection in a partial scan design can be characterized by the following criteria:

1) Test Generation Based Approach
2) Structural Analysis Based Approach
3) Testability Analysis Based Approach

The main factors that distinguish all these approaches is that whether it uses sequential or combinational test generators, whether it is separate from test generation process or integrated with it and the testability figures achieved by these different techniques. In this section, these approaches are briefly discussed along with their advantages, potentials and shortcomings.

Test generation based approach, proposed by [2], focuses on the simplification of test pattern generation. In this approach, partial scan analysis is separated from the test generation and relies on the modified combinational test generator (CTG) which is described in their paper as the modified PODEM algorithm. During the partial scan analysis, the most probable candidate flip-flops to be included in the scan chain are recorded. The frequency based approach for partial scan analysis presented in [1] makes use of Extended PODEM algorithm, which instead of generating one test for a given fault, produces a set of all the possible tests for that fault. The inputs of those flip-flops that are not part of the scan chain are set to don't-cares. This techniques relies on the fault coverage achieved by the functional test vectors, generated during design verification process. The faults that are not detected by functional test vectors are target by partial scan and it is assumed that test pattern generators is able to produce test for all the components that are part of the partial-scan design. This approach works as follows:

1) For every fault in the fault list, generate all the possible test sequences to test the fault. These test sequences specify the usage of the flip-flops for that particular fault.

2) For every fault in the fault list, it determines the corresponding frequency of usage of every flip-flop specified by the test sequences.

3) The flip-flop with the highest frequency is included the scan chain.

4) If there is any fault in the fault list that can be covered by the flip-flops in the scan list, that fault is removed from the fault list and that particular test sequence among all possible ones, which can be applied to test that particular fault using available scan flip-flops, is selected.

5) This process is repeated and more flip-flops are added in the scan list until the fault list is empty. It also calculates the estimated fault-coverage, using an empirical formula given in the paper, that can be attained by using the partial-scan using only those flip-flops that are in the scan list.

The partial scan chain is made of only those flip-flops that are in the scan list. The practical fault coverage obtained this partial scan technique is claimed to be close to the theoretical limit given by the empirical formula. The fault coverage figure is sensitive to the fault coverage that is achieved by the functional test vectors, without using any scan methodology. The algorithm is flexible and lets the designer choose among the several options, specifying different number of scan flip-flops and corresponding fault coverage.

This technique simplifies the ATPG process and make it possible to use CTG for testing sequential circuits, assuming that sequential and combinational parts of design can be isolated and faults can be mapped onto combinational part. But this technique is only applicable to the sequential circuit with no loop-backs, including the self loops, something that is hard to see in sequential circuits. Therefore, it is required that S-graphs of sequential circuits are reduced such that they are free of any loops. Removing self-loops can be very expensive since sequential circuits have very large number of self loops in general.

Structural Analysis is another approach for partial scan analysis proposed by the [3]. It is based on the observation that for the STG that uses time frame expansion to generate the test sequences, the major problem is posed by the loops in the S-graph representing the sequential circuit. In S-graph, vertices represent the flip-flops and the edges represent combinational parts of the circuits. If the depth of S-graph D is defined as largest number of flip-flops from input to output and L is length of largest feedback loop which is formed when output of a flip-flop is fed back to its input after passing through combinational circuit and/or other flip-flops as well, then the test sequence length is approximated as D*2L. The approach presented by the authors is to break the major loops in the graph, except for the self loops (loops for which L=1), so that the graph becomes acyclic. Such graph can easily be handled by a STG regardless of its sequential depth. The idea of making the graph acyclic, neglecting the self loops, revolves around finding the best flip-flops that can break the loops. There can be multiple cycles in the graph, i.e., cycles embedded in other cycles. Therefore the best flip selection is made for the one that will break the inner loop. The reason is that if the inner cycle is broken, the outer cycle which previously contained that inner cycle will automatically break. For example, in Figure 5, cycle[3,4,5] is embedded in the outer cycle[1,2,3,4,5,6], and breaking of the inner cycle will automatically break the outer one. The algorithm for cycle breaking is then about selection of minimum number of flip-flips that will remove all the major loops in the graph. In this algorithm, first a cycle list is constructed from the net list description of circuit. This cycle list records all the flip-flops making the cycles. This cycle list contains only those cycles which contain no inner cycles for the reasons explained above. For breaking of loops, sequence of steps is as follows:

1) Generate cycle list containing all cycles in the graph with no inner cycles

2) Count frequency of appearance of a flip-flop in the cycle list

3) Put the flip-flop with highest frequency in the scan flip-flop list and remove all the cycles containing that flip-flop

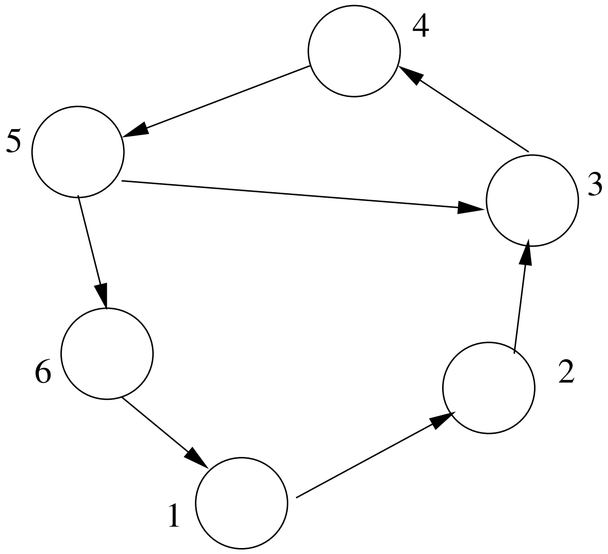

Figure 5. Directed S-Graph of sequential circuit

his process is repeated until all the cycles, except for the self loops, are removed. Removal of self loops can be very expensive computational efforts as sequential designs usually have a very large number of self loops and secondly such loops do not cause major problem for ATPG process.

Separate clocks are used during the normal and scan mode. Also separate STG and fault simulator are used for the test sequence generation for given fault list. It is shown that for almost 5

The major drawback of such schemes is that faults in the flip-flops that are not included in the scan chain cannot be detected and that the quality of the selection process is not guaranteed. The order in which the flip-flops are selected is greatly influenced by the order in which the target faults are specified.

Testability Analysis [1, 4, 7], approach guarantees to attain the desired fault coverage for partial scan design. The basic idea behind almost all approaches based on testability analysis is that the flip-flops that are not included in the scan chain cannot be controlled and observed. Therefore the faults in those flip-flops cannot be detected. In order to assure the quality of selection process, effect of each flip-flop on the overall testability of the circuit is calculated using some exact method or by a heuristic. The flip-flops that give the highest improvement in the testability are included in the scan chain. The theoretical complexity of all such algorithms is of O(n2) where n is the number of flip-flops. One such algorithm, PASCAL [1], ranks all the FF according to their based on their contribution to the fault coverage. Algorithm can either be implemented by starting from non-scan design and adding one FF of highest rank each time in the scan chain or from full scan design and deleting one FF with lowest rank each time. PASCAL is implemented using second approach, although both are equivalent. In this algorithm, a FF is temporarily removed from the chain. Its input is now uncontrollable and output is unobservable. The effect on testability is recorded by propagating uncontrollabilities forward and unobservabilities backwards and calculating resulting undetectable faults. (It is shown that generally, if the gate input cannot be set to the non controlling value of the gate, all the other inputs become unobservable. The unobservability propagates from the gate output backward to its inputs).The FF is inserted back and the process is repeated for all the FF. Once the best FF is found, the one which introduces minimum number of undetectable faults, is removed from the scan chain permanently. The process is repeated on remaining n-1 number of flip-flops until desired fault coverage is achieved or some other termination criteria (e.g. time limit) is met. Number of flip-flops in the scan chain (and also computation time) can be reduced by not including those FF in analysis that are in the critical path. Tests are generated using CTG. All those faults that are undetectable or targeting only those faults which are not detected by functional test sequences can improve the performance of the algorithms. A similar approach is suggested in [4].

All the approaches discussed above are some of those that are in use for partial scan selection problem. More recent papers suggest new algorithms like Circuit State Information, Valid State Analysis, Dynamic Reachability and Observability which are discussed in detail in [8, 9, 5, 10]. Some of these techniques claim almost 100

4. Delay testing in partial scan

Testing VLSI sequential circuits under simple fault models such as the single stuck-at-fault model is itself a difficult task. Testing sequential circuits for delay faults is an even more challenging problem. Detecting a path delay or gate delay fault in an integrated circuit requires the application of a vector pair, with the circuit being clocked at speed after the application of each vector. To test delay faults, two test vector patterns have to be applied in order to generate the transition to be tested. The test is composed of two test vectors: an initialization vector and an activation vector. The initialization vector is first applied, and maintained for some time so that the gates have time to settle. Then, the activation vector is applied, and the result is sampled after one clock cycle. Very low fault coverage is obtained if only the primary inputs or outputs are available. To solve this problem, scan registers are inserted in the chip, which decreases the complexity of delay, faults detection. The initialization vector is scanned in a register and is then applied to the circuit. The activation vector is then applied by loading functional outputs obtained after the application of initialization vector. The result of the transition is loaded in a scan register after one clock cycle and is then scanned out. The second vector has to be deducted from the first vector and is therefore to be chosen from a very restricted number of vectors. An alternative is that the activation vector is a 1 bit shifted version of the initialization vector. Hence standard scan design does not allow for the application of arbitrary vector pairs. The advantage of these methods is that the delay fault testing does not require additional area overhead, but the number of test patterns become very limited. As a result, to apply the necessary vector pair for delay testing, the circuit may have to be implemented with enhanced-scan flip-flops that can store two bits of state, and using these flip-flops can result in a significant area overhead. The procedure is that the initialization vector is scanned in the register and is applied to the functional block. When the functional block is initializing, the activation vector is scanned in the register. When the activation vector is totally in the register, it is applied to the functional block, and the result is obtained in a scan register after one clock cycle and is then scanned out. The advantage of this approach is that the test-vector pairs can be chosen freely but as already mentioned above, it requires a large area over head. Two of the major costs of delay-fault testing are the area overhead incurred by enhanced-scan flip flops and the additional test time required to apply large vector sets.

4.1. Partial Scan Circuits

Similar to stuck-fault test generation, the complexity of test generation for delay faults may be too high for large circuits or for circuits with a complex structure. For stuck-faults, partial scan is a viable DFT technique for reducing the computati onal complexity of test generation to a manageable level. However, the normal test application scheme for partial scan circuits does not apply patterns to the combinational portion of the sequential logic at speed and, thus, cannot detect delay faults. Some changes on test application must be made for detecting delay faults.

A typical test application scheme for partial scan circuits is as following:

1. Set the circuit in test mode.
2. Scan in the required state.
3. Change the circuit mode into normal mode.
4. Apply one vector to the primary inputs followed by a system clock.
5. Scan out.

Because scanning in a state takes several clock cycles, the time interval between the applications of two input vectors to the combinational portion of the sequential logic will be too long to detect delay faults.

The input sequence is specified as a set of subsequences each of which is used to detect some delay faults. The first vector of a subsequence consists of two parts: primary input part and scan input part, which is also called initial state. The other vectors in the subsequence are only specified at the primary inputs. A separate scan clock is used for scan. Suppose the input sequence consists of k subsequences, each of which has a length of Lj , j = 1,2,.k. The procedure for applying the i-th subsequence is:

1. Scan in the initial state. Take n scan clock cycles.
2. Set the circuit in the test mode
3. Repeat Li-1 times
   a. Apply an input vector
   b. Apply a system clock
   c. Scan one more bit
4. Set the circuit in the normal mode
5. Apply vector VL
6. Apply a system clock
7. Scan out / Scan in next initial state.

For a partial scan circuit, the inputs to the combinational logic can be divided into three categories: primary inputs (PI), the outputs of Scan flip-flops (SI) and the outputs of non-scan flip-flops (called present state line, PS). For the application scheme given in Fig. The values at SIs are obtained by the single bit shift of the scan register (step 3.c). This is done by holding the mode

switch in the test mode and using the scan clock for scan. The values at the PSs

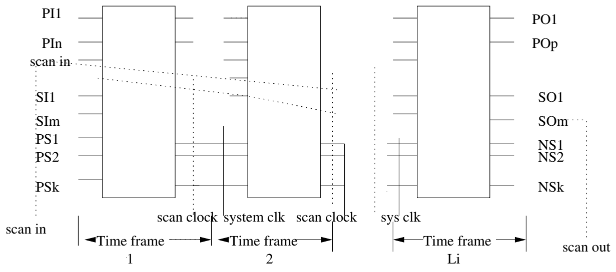

Figure 6. Test application for partial scan circuit

are the values at the next state lines (denoted as NS) in the previous cycle, which are latched by the system clock. It should be noted that inside loop 3. the circuit is kept in the test mode and, thus a scan flip flop will not be able to latch a fault effect even if a fault effect is already appears at the scan

flip-flops data input. Fault effects can be latched in the scan flip-flops

in step 6. The faults can be detected at any vector if a fault effect appears at a primary output. The time interval between the applications of two vectors to the combinational logic is limited by the time required to perform Steps 3.1 and 3.3 can be overlapped in time.

For this application scheme, the test sequences must be carefully designed to be able to obtain high transition fault coverage.

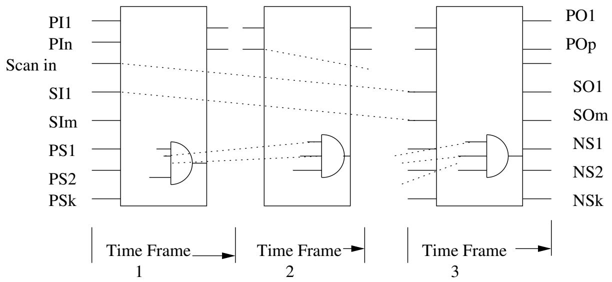

Figure 7. Test generation model

Figure shows the test generation model for partial scan circuits. There are n primary inputs , m scan flip-flops, k non-scan flip-flops and p primary outputs. We start from the last time frame- time frame N. All primary outputs (POs), pseudo outputs (SOs i.e. the data inputs of the scan flip-flops) and next state lines (NSs) are assumed fully observable and the above algorithm is used to justify D or D at a selected primary output. In a backward justification, if a value is assigned to SIi in a time frame x, the value needs further justification and is assigned to SIi-1 in time frame x-1 (as shown in dashed lines in fig.). It is assumed that the scan flip-flop I-1 is the predecessor of scan flip-flop in the scan register. Test generation is completed when no required state is specified in the present state lines (PSs) as well as the first k inputs of the inserted states. A scan-in sequence will be added at the beginning of the sequence to produce

the required initial values at SIs. Fault simulation is then followed to remove faults detected by the new sequence. During fault simulation, SOs are not observable from time frame 1 to time frame N-1. This is because the circuit is set to the test mode in these time frames so that the scan flip-flops will not latch values from their data inputs in these time frames. The SOs are observable at

time frame N.In fault simulation, the final value at each signal produced by the previous test sequence cannot be used as the initial value for the newly generated sequence. This is because the scan sequence has been inserted between two test sequences. If we set the system clock inactive during scanning, the final states of

previous test sequence can be used as the initial states for the new test sequence. However, because the values at the primary inputs and pseudo inputs keep changing during scan, it is assumed that the initial values at all other signals are unknown.

The order of flip-flops placed in the partial scan chain will affect the fault coverage. Some faults that are testable under one order may become untestable in another order.

5. Summary

In this paper we discussed about partial scan design technique and the effect of path delays in perspective of IEEE 1149.1. We realized that due to remarkable increase of transistors on chip level and complex structures are bottlenecks in implementing cost effective testing.In such cases One can not rely on traditional techniques;partial scan could be one of the most attractive technique for complex circuits while minimising the delays and reducing the area.

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