Solution to supplementary problems.

Problem 15

The question could have formulated as follows: *How may the fraction B, $B = \frac{W_p}{W_n}$, be chosen, such that the average delay is minimised using a constant area:*

$$t_{inv} = k\,(R_n + R_p)\,C_{eq} = \left(1 + \frac{\mu_n}{\mu_p}\,\frac{1}{B}\right)(1+B)\tau_{eq}$$

$$\frac{dt_{inv}}{dB} = \left(1 - \left(\frac{\mu_n}{\mu_p}\right)\frac{1}{B^2}\right)\tau_{eq} \qquad \frac{dt_{inv}}{dB} = 0 \Leftrightarrow B = \sqrt{\frac{\mu_n}{\mu_p}}$$

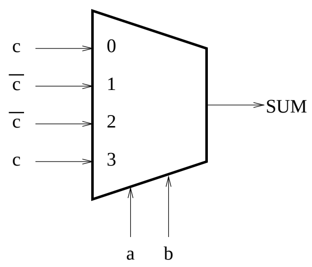
Problem 16

The pass-transistor circuit may be realised using a $(n-1)^2 : 1$ multiplexor, where n is the number of variables in the function.

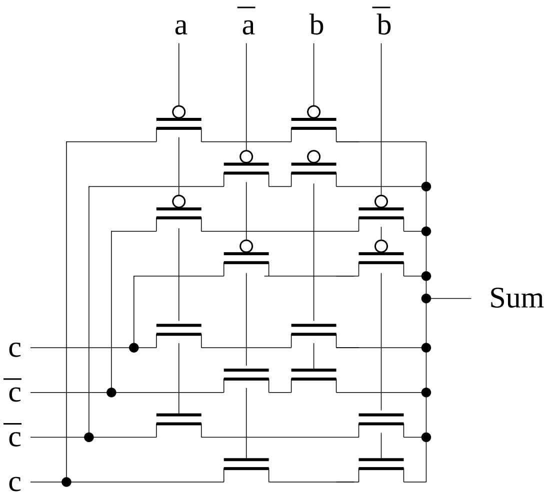
c \ ab	00	01	11	10
0	0	1	0	1
1	1	0	1	0

c \ ab	00	01	11	10
0	c	$\overline{c}$	c	$\overline{c}$
1	c	$\overline{c}$	c	$\overline{c}$

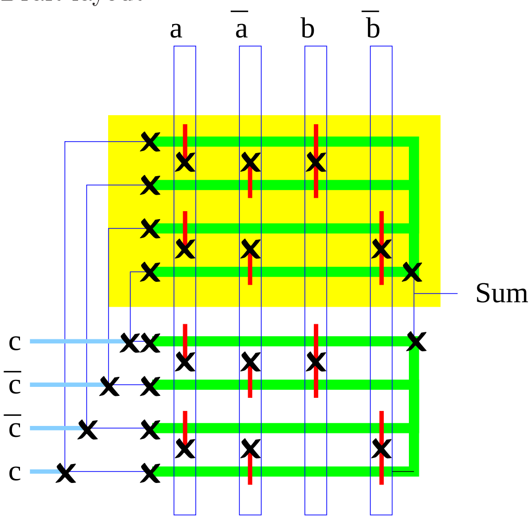
Sketch



Transistor diagram



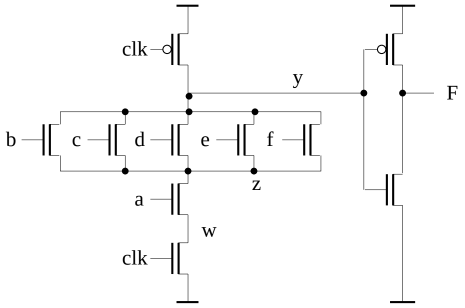
Draft layout



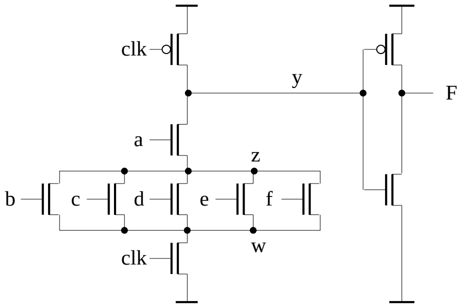
Problem 17

1. Transistor diagrams

Realisation A



Realisation B



2. The gate threshold of the inverter at the output is calculated using Formula (2.24) and inserting values of the current gain factor ($\beta = KP(\frac{W}{L})$)

$$V_{kip} = \frac{V_{DD} + V_{tp} + V_{tn}\sqrt{\frac{KP_n}{KP_p}}}{1 + \sqrt{\frac{KP_n}{KP_p}}} = \frac{1.8 - 0.47 + 0.48\sqrt{\frac{265}{78.7}}}{1 + \sqrt{\frac{265}{78.7}}} V = 0.770V$$

3. The circuit may fail during evaluation, when y is 1, i.e. when the pull-down network is not conducting. The error occurs if the voltage on node y due to charge redistribution of the charges on nodes y and z incorrectly drops below V_{kip}. Thus, the charge on w is not part of the problem.

   The sequence of inputs, that provokes the faulty response, must

   (a) at first discharge nodes z and w,

   (b) precharge node y, without recharging node z,

   (c) evaluate, such that nodes y and z but not w are connected

   Realisation A

clk	a	b+c+d+e+f	y	z	w	F
1	1	X	X	0	0	X
0	0	0	1	0	0	0
1	0	0	1	0	0	0
1	0	1	?	?	0	?

   Realisation B

clk	a	b+c+d+e+f	y	z	w	F
1	X	1	X	0	0	X
0	0	0	1	0	0	0
1	0	0	1	0	0	0
1	1	0	?	?	0	?

4. The capacitances on nodes y and z:

   n-type diffusion capacitance, C_n :
   $C_n = A_n \cdot C_{jn} + P_n \cdot C_{jnp} = 0.28 \cdot 0.4 \cdot 1243aF + 2(0.28 + 0.4) \cdot 10.7aF = 154aF$

   p-type diffusion capacitance, C_p :
   $C_p = A_p \cdot C_{jp} + P_p \cdot C_{jpp} = 0.28 \cdot 0.4 \cdot 958aF + 2(0.28 + 0.4) \cdot 35.8aF = 156aF$

   Gate capacitance, C_g :

$$C_g = L \cdot W \cdot C_{ox} = 0.18 \cdot 0.28 \cdot \frac{3.9 \cdot 8.85pF}{3.2n} = 544aF$$

   Realisation A

$$\begin{aligned} C_y &= 2C_g + C_p + 3C_n = 1.71fF \\ C_z &= 3C_n = 462aF \\ V_y &= \frac{C_y}{C_y + C_z} V_{dd} = \frac{1.71}{1.71 + 0.462} \cdot 1.8V = 1.42V \end{aligned}$$

4. continued:

<u>Realisation B</u>

$$\begin{aligned} C_y &= 2C_g + C_p + C_n = 1.40fF \\ C_z &= 3C_n = 462aF \\ V_y &= \frac{C_y}{C_y + C_z} V_{dd} = \frac{1.40}{1.40 + 0.462} \cdot 1.8V = 1.35V \end{aligned}$$

5. In each case, $V_y > V_{kip}$, and neither circuit fails. Static noise margins are reduced, and the voltage drops are large enough to make the inverter consume static power. The analysis did not consider wire capacitances, nor the voltage dependent diffusion and gate capacitances. All wire capacitances should be extracted from layout to permit a more detailed analysis. Finally, variations in V_{tn}, V_{tp}, KP_n, KP_p and V_{DD} may influence the inverter threshold, V_{kip}, of the output inverter.

Problem 18

In this problem, we are free to choose the number of buffer stages, n, and the ratio of W_p and W_n for each stage. The input capacitance, C_{in}, consists of two gate capacitances. The delay of an inverter loaded by a similar inverter is determined using Formulas (4.44-45) inserting $k = 4$:

$$C_{ox} = \frac{\epsilon_{r,SiO_2}\epsilon_0}{t_{ox}} = \frac{3.9 \cdot 8.85pFm^{-1}}{32} = 10.8fF(\mu m)^{-2}$$

$$C_{in} = 2 \cdot W \cdot L \cdot C_{ox} = 2 \cdot 0.18 \cdot 0.28 \cdot 10.8fF = 1.09fF$$

$$t_{dx} = \frac{1}{2}\frac{k \cdot C_L}{KP_x \cdot V_{DD}}\frac{L}{W} = 4\frac{L \cdot W \cdot C_{ox}}{KP_x \cdot V_{DD}}\frac{L}{W} = \frac{4L^2 \cdot C_{ox}}{KP_x \cdot V_{DD}}$$

$$\left.\begin{aligned} t_{dr} &= \tfrac{4L^2 \cdot C_{ox}}{KP_p \cdot V_{DD}} = \tfrac{4 \cdot 0.18^2 \cdot 10.8fF}{78.7\mu A/V^2 \cdot 1.8V} = 9.9ps \\ t_{df} &= \tfrac{4L^2 \cdot C_{ox}}{KP_n \cdot V_{DD}} = \tfrac{4 \cdot 0.18^2 \cdot 10.8fF}{265\mu A/V^2 \cdot 1.8V} = 2.9ps \end{aligned}\right\} \quad t_d = \frac{1}{2}(t_{dr} + t_{df}) = 6.4ps$$

In the following, several differently dimensioned drivers are discussed:

The fastest driver

First, the fastest solution is explored. Formulas (4.64-65) are used with $k = 0$, i.e. the optimal buffer ratio is e. $W_p = W_n$ is chosen in all stages:

Number of stages: $n = \log \frac{C_L}{C_{in}} = \log \frac{50pF}{1.09fF} = 3.8$
Step-up factor: $a = e$
Delay: $\tau = n \cdot a \cdot t_d = 4e \cdot 6.4ps = 69.6ps$
Thus, the requirement $\tau < 5ns$ is easily met. Therefore, choosing fewer steps, corresponding to a larger step-up factor, is possible.

A driver with minimum number of stages

$$\tau = \frac{a}{\log a} \log \frac{C_L}{C_{in}} t_d \quad \Leftrightarrow \quad \frac{a}{\log a} = \frac{\tau}{t_d \log \frac{C_L}{C_{in}}}$$

$$\frac{a}{\log a} \leq \frac{5ns}{6.4ps \log \frac{50pF}{1.09fF}} = 185.4 \quad \Leftrightarrow \quad a \leq 1334$$

Number of stages: $n = \frac{\log \frac{C_L}{C_{in}}}{\log a} = 0.7 \quad \rightsquigarrow \quad$ 1 stages are necessary
Step-up factor: $a^1 = \frac{C_L}{C_{in}} \Leftarrow a = 46$
Delay: $\tau = 2 \cdot 46 \cdot 6.4ns = 0.589ns$
Note: the driver is not symmetrical with respect to rise and fall times.

Yet another driver: a 3-stage driver

Last, a 3-stage driver with symmetrical rise and fall times is considered. The first and second inverters both have $W_p = W_n$, i.e. rise and fall times are equal for the inverter pair. The second inverter is sized with the step-up factor a, such that $t_{d1} + t_{d2} = 0.5ns$. The output inverter is dimensioned to have $t_{d3} = 4.0ns$, leaving a design margin. Further, the transistors are matched ($W_p = \frac{KP_n}{KP_p} W_p$) to achieve equal rise and fall times for the inverter.

Stage 3:

$$\begin{aligned} t_{dr} &= \frac{2C_L}{KP_p V_{DD}} \frac{L}{W_p} \Rightarrow W_p = \frac{2C_L \cdot L}{t_{dr} KP_p V_{DD}} \\ W_p &= \frac{2 \cdot 50pF \cdot 0.25\mu m}{4.0ns \cdot 60\mu A/V^2 \cdot 2.5V} = 41.5\mu m \\ W_n &= \frac{60\mu A/V^2}{263\mu A/V^2} 41.5\mu m = 9.5\mu m \end{aligned}$$

Stage 2:

$$\begin{aligned} C_{g3} &= (W_{p3} + W_{n3}) \cdot L \cdot C_{ox} = (41.5 + 9.5) \cdot 0.25 \cdot 6.9fF = 88.0fF \\ a^2 &= \frac{C_{g3}}{C_{in}} \Rightarrow a = \sqrt{\frac{88.0}{1.73}} = 7.13 \\ W_{p2} &= W_{n2} = a \cdot W_{p1} = 7.13 \cdot 0.5\mu m = 3.5\mu m \end{aligned}$$

Stage	W_p μm	W_n μm	C_g fF	C_d fF	t_{dr} ps	t_{df} ps
1	0.5		1.73	0.99	87	20
2	3.5		12.11	4.96	826	188
3	41.5	9.5	88.0	32.63	4109	4095

Note that $t_r = t_f = 2 \cdot 4.1ns = 8.2ns$. In the following calculations, the 'final' driver design is used.

1. The power consumption of the driver is

$$\begin{aligned} P_{buf} &\simeq P_d(\text{Stage 1-3}) + P_{sc}(\text{Stage 3}) \\ P_d &= (C_{L1} + C_{L2} + C_{L3}) V_{DD}^2 f_p \\ &= (C_{d1} + C_{g2} + C_{d2} + C_{g3} + C_{d3} + C_L) V_{DD}^2 f_p \\ &= 52152fF \cdot (2.5V)^2 \cdot 100MHz = 32.6mW \\ P_{sc} &= \frac{\beta}{12}(V_{DD} + V_{tp} - V_{tn})^3 \frac{t_{rf}}{t_p} \\ &= \frac{263\mu A/V^2}{12} \frac{9.5}{1} (2.5V - 0.55V - 0.56V)^3 \frac{8.2ns}{10ns} = 459\mu W \\ P_{buf} &\simeq 33mW \end{aligned}$$

16 buffers will draw an average current of

$$I = \frac{16P_{buf}}{V_{DD}} = \frac{16 \cdot 33mW}{2.5V} = 211mA$$

2. The current through a $120\mu m$ wide metal-6 wire is determined by the maximum current density, J_{M6}:

$$I = J_{M6} \cdot W = 1.96mA/\mu m \cdot 120\mu m = 235mA$$

A single pair of V_{DD} / V_{SS} pads suffices.

Problem 19

The dynamical power consumption, P_d, is calculated using Formula (4.70)

$$P_d = C_L \cdot V_{DD}^2 \cdot f_p = 300pF \cdot (1.8V)^2 \cdot 450MHz = 437mW$$

The short circuit consumption, P_{sc}, can not be calculated without knowing the structure of the circuit (not mentioned in the text). In the reply, I assume, that the 300pF above results from 141500 inverters of size $(W_p; W_n; L) = (0.56\mu m; 0.28\mu m; 0.18\mu m)$. The figure (141500) is derived from estimating the capacitance of an inverter:

$$\begin{aligned}
C_g &= (W_p + W_n)LC_{ox} = (0.56 + 0.28) \cdot 0.18 \cdot 10.8fF = 1.63fF \\
C_d &= A_nC_{jn} + P_nC_{jnp} + A_pC_{jp} + P_pC_{jpp} \\
&= 0.4 \cdot 0.28 \cdot 1243 + 2(0.4 + 0.28)10.7 + \\
&\quad 0.4 \cdot 0.56 \cdot 958 + 2(0.4 + 0.56)35.8 = \qquad 491aF \\
n &= \frac{C_{total}}{C_g + C_d} = \frac{300pF}{(1.63 + 0.491)fF} \approx \quad 141500
\end{aligned}$$

$t_{rf} = 25ps$ is given, and P_{sc} may now be calculated using Formula (4.72):

$$\begin{aligned}
P_{sc} &= n \cdot \frac{\beta}{12}(V_{DD} + V_{tp} - V_{tn})^3 \cdot \frac{t_{rf}}{t_p} \\
&= \frac{141500 \cdot 78.7\mu A/V^2}{12}\frac{0.56\mu m}{0.18\mu m}(1.8V - 0.47V - 0.48V)^3 \cdot \frac{25ps}{5ns} \\
&= 8.9mW \qquad \text{or 2\% of the total power consumption}
\end{aligned}$$

When $V_{DD} = 1.2V$, $P_{sc} = 226\mu W$. $t_{rf} = 150ps$ results in $P_{sc} = 53.4mW$. In the later example, P_{sc} accounts for as much as 12% of the total power consumption.