Solution to supplementary problems.

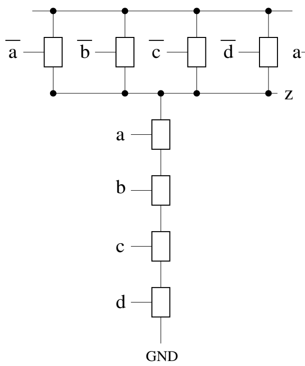
Problem 1

a) $z = \overline{a \bullet b \bullet c \bullet d}$ (NAND)

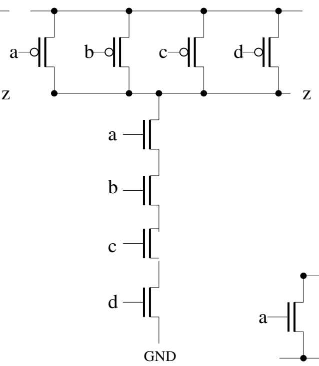
1) $z = \overline{a} + \overline{b} + \overline{c} + \overline{d}$

$\overline{z} = a \bullet b \bullet c \bullet d$

2) Switch network



3) Transistor diagram

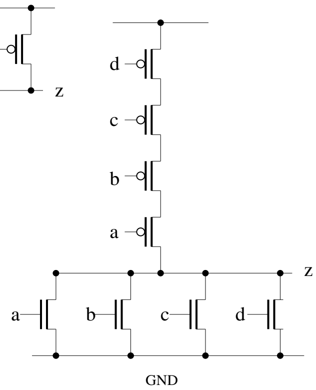


b) $z = \overline{a + b + c + d}$

$z = \overline{a} \bullet \overline{b} \bullet \overline{c} \bullet \overline{d}$

$\overline{z} = a + b + c + d$

3) Transistor diagram



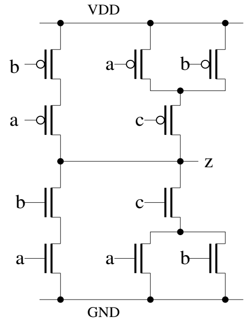
c) $z = \overline{a \cdot b + c \cdot (a + b)}$

$z = \overline{a} \cdot \overline{b} + \overline{c} \cdot (\overline{a} + \overline{b})$

$\overline{z} = a \cdot b + c \cdot (a + b)$

c \ ab	00	01	11	10
0	1	1	0	1
1	1	0	0	0

3) Transistor diagram



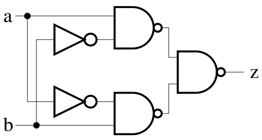
Problem 2

a) $z = a \cdot \overline{b} + \overline{a} \cdot b$ (EXOR)

1) $z = a \cdot \overline{b} + \overline{a} \cdot b$

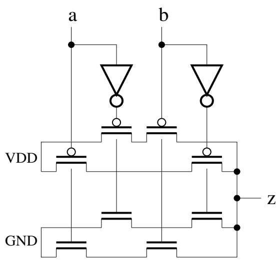
$\overline{z} = \overline{a} \cdot \overline{b} + a \cdot b$

2) Gate realisation



(16 transistors)

3) Transistor realisation



(12 transistors)

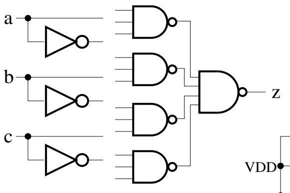
Note: the structure is programmable

b) $z = a \cdot \overline{b} \cdot \overline{c} + \overline{a} \cdot b \cdot \overline{c} + \overline{a} \cdot \overline{b} \cdot c + a \cdot b \cdot c$

Possible solutions

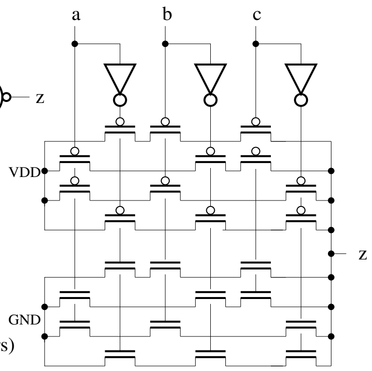
1) Use 2 EXOR gates as constructed under 2b
24 transistors

2) Gate realisation



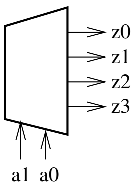
(38 transistors)

3) Transistor realisation

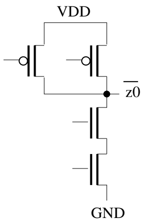


(30 transistors)

Problem 3

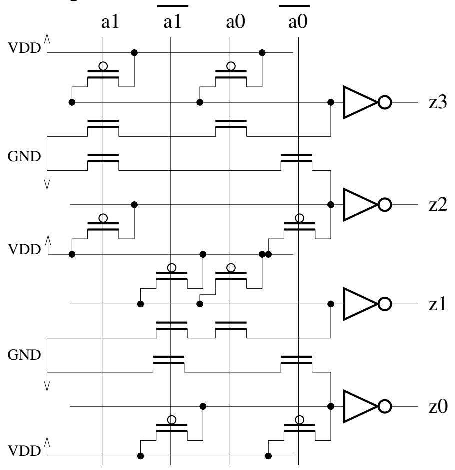


a1	a0	z3	z2	z1	z0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

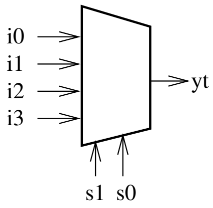


Electrically, a NAND gate is prefered!

Transistor diagram

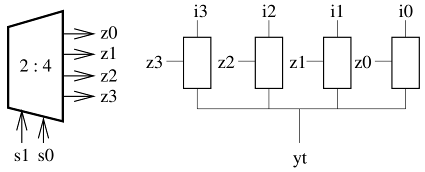


Problem 4

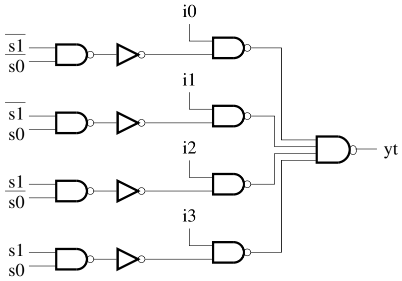


s1	s0	yt
0	0	i0
0	1	i1
1	0	i2
1	1	i3

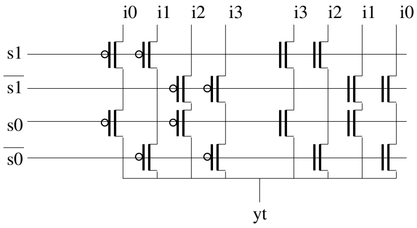
Solution 1:



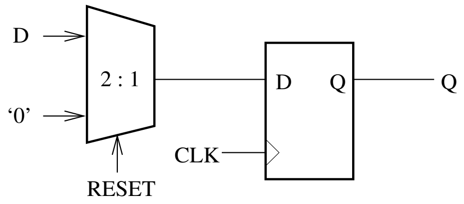
Solution 2:



Solution 3:

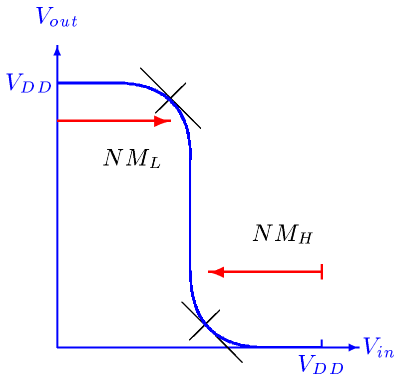


Problem 5



Multiplexor of Problem 4, D flipflop of N. Weste, Figure 1.13

Problem 6



Under the stated conditions ($V_t = V_{tn} = -V_{tp}$, $\beta_n = \beta_p$), the electrical strengths of the transistors are equal. Therefore, the DC transfer characteristic of the inverter must be symmetrical about $(\frac{V_{DD}}{2}, \frac{V_{DD}}{2})$. This applies to the unity gain points and noise margins as well. Thus, $NM = NM_L = NM_H$.
One unity gain point can be determined using Formula (2.23) expressing the DC transfer function for a saturated, n-channel MOS transistor. Similarly, Formula (2.27) can be used to determine the other unity gain point:

$$\begin{aligned}
\frac{\partial V_{out}}{\partial V_{in}} &= 1 + \frac{2(V_{in} - V_{tp}) - 2V_{DD} - 2\frac{\beta_n}{\beta_p}(V_{in} - V_{tn})}{2\sqrt{(V_{in} - V_{tp})^2 - 2(V_{in} - \frac{1}{2}V_{DD} - V_{tp})V_{DD} - \frac{\beta_n}{\beta_p}(V_{in} - V_{tn})^2}} \\
\frac{\partial V_{out}}{\partial V_{in}} &= -1 \Leftrightarrow \\
0 &= V_{DD} - (\frac{\beta_n}{\beta_p}V_{tn} - V_{tp}) + (\frac{\beta_n}{\beta_p} - 1)V_{in}) - 2\sqrt{(V_{in} - V_{tp})^2 - 2(V_{in} - \bullet\bullet\bullet}
\end{aligned}$$

Inserting $V_t = V_{tn} = -V_{tp}$ and $\frac{\beta_n}{\beta_p} = 1$ simplifies the expression to

$$\begin{aligned}
V_{DD} - 2V_t &= 2\sqrt{(V_{DD} - 2V_t)(V_{DD} - 2V_{in})} \Rightarrow \\
V_{DD} - 2V_t &= 4(V_{DD} - 2V_{in}) \Leftrightarrow \\
V_{in} &= \frac{3}{8}V_{DD} + \frac{1}{4}V_t
\end{aligned}$$

The operating points are $V_{OL,max} = V_{SS}$ and $V_{OH,min} = V_{DD}$, respectively. By definition, $V_{IL,max}$ has been determined. By symmetry, $V_{IH,min} = \frac{5}{8}V_{DD} - \frac{1}{4}V_t$:

$$(V_{IL,max}, V_{IH,min}, V_{OL,max}, V_{OH,min}) = \begin{cases} (\ 794mV\ ;\ 1.01V\ ;\ 0V\ ;\ 1.8V\ )_{V_{DD}=1.8V} \\ \\ (\ 569mV\ ;\ 631mV\ ;\ 0V\ ;\ 1.2V\ )_{V_{DD}=1.2V} \end{cases}$$

The noise margins are:

$$NM_L = NM_H \quad = \quad 794\ mV\ |_{V_{DD}=1.8V} \quad \text{and} \quad 569\ mV\ |_{V_{DD}=1.2V}$$

The noise margins may be improved by adjusting V_{DD} and/or V_t. Both noise margins are improved by increasing V_t.
Alternatively, one noise margin may be improved at the expense of the other. E.g. NM_L can be improved at the expense of NM_H by changing the gate threshold of the inverter, V_{KIP}.