Problem 18: Design of output buffer

Design an output buffer that will buffer an external load of 50pF in 5ns. The internal driver has W_p=W_n=0.5μm, L_p=L_n=0.25μm. V_{DD}=2.5V:

1. Calculate the current drawn by 16 such buffers that are simultaneously driven at a clock rate of 100 MHz
2. Determine the number of power and ground pads necessary for the 16 buffers, when the length of the V_{DD} and V_{SS} to each pad is 120μm

Problem 19: Power dissipation

Calculate the approximate dynamic and short-circuit power dissipated in a chip operating with a V_{DD} of 1.8V at 450MHz with an internal switched capacitance of 300pF, assuming that the average rise/fall time is 25ps.
Calculate the approximate dynamic and short-circuit power dissipated in the same chip, when V_{DD} is 1.2V Determine the short-circuit dissipation change when the average rise/fall time is 150ps.

Problem 20: Worst-Case and Best-Case Delay Times

Process tolerances and variations in temperature and supply voltages have a strong influence on delay times in integrated circuits. Usually, the semiconductor manufacturer supplies 3 sets of SPICE parameters labeled '*Typical*', '*Slow*' and '*Fast*'. Worst-case and best-case delay times may be calculated using these sets of parameters, inserting appropriate values for supply voltage, V_{DD}, and junction temperature, T_j.

The delay of a (combinational) circuit is (approximately):

$$t_d = 2\frac{C_L}{KP \cdot V_{DD}}\left(\frac{l}{w}\right) \qquad KP = \frac{\mu \cdot \epsilon}{t_{ox}}$$

Variations in process or temperature affect the mobility, μ, whereas little or no effect is seen on ϵ and t_{ox}. For a specific CMOS process, the manufacturer states the following[1]:

- Process variations: Values of KP at $T_j = 300K$:

KP_N [μA/V^2]	Min	239.	Typ	265.	Max	292.
KP_P [μA/V^2]		71.0		78.7		86.8

- Temperature variations: $KP[T] = KP[T_0] \cdot \left(\frac{T}{T_0}\right)^{-1.54}$

Now assume, that you have constructed a circuit and determined the delay times using: (1) typical process parameters, (2) $T_a = T_j = 300K$ and $V_{DD} = 1.8V$. The circuit is part of an IC with an estimated power consumption of 4.0 W. The IC will be mounted in a package with $\Theta_{ja} = 35\ ^o$C/W. The temperature conditions specified for the IC are:

Ambient temperature: $0\ ^o\text{C} < T_a < 70\ ^o\text{C}$
Supply voltage: $1.2V < V_{DD} < 1.8V$

1. Determine the relative change in delay times for '*worst-case*' and '*best-case*' respectively.
2. In the analysis, only variations in KP, V_{DD}, and T_j are considered. Name at least two more factors, which influence delay time and must be taken into consideration in a more detailed analysis.

[1] Refer to N. Weste Section 2.2.2.4 and Formula (2.30)

Problem 21: Calculation of Cross Capacitances

Upper plate	Lower plate poly-Si	Metal-1	Metal-2	Metal-3	Metal-4	Metal-5
Metal-1						
Metal-2						
Metal-3						
Metal-4						
Metal-5						
Metal-6						

Use the geometrical design rules and electrical parameters from the design rules[1] to fill in the blanks of the table above, i.e.

1. Calculate the distance between any pair of two layers (poly-silicon, metal-1 through metal-6).
2. Calculate the capacitance between any two layers (poly-silicon, metal-1 through metal-6), assuming that the capacitors can be considered as plate capacitors.
   The relative permittivity is constant, $\epsilon_r = 3.9$.

Problem 22: Estimate of Routing Capacitances

In a rectangular area, signals are routed using metal wires of minimum conductor line widths in layers metal-2, metal-3, metal-4 and metal-5. Layers metal-2 and metal-4 are run in parallel, perpendicular to layers metal-3 and metal-5. The wires of layers metal-2, metal-3, and metal-4, are placed on a $0.64\mu m$ grid, whereas wires of layer metal-5 are placed on a $1.28\mu m$ grid.

Routing capacitances are estimated under the assumptions that capacitances can be approximated as plate capacitors with no edge contributions, and that signals are routed, and thus loaded, as:

- the metal-6 layer is filled to 35%,
- capacitances to layers above metal-6 can be ignored,
- in metal-2 through metal-5 layers, 50% of all grid positions are filled,
- the contribution from vias to the cross capacitances can be ignored,
- the metal-1 layer is filled to 35%,
- the poly-Si layer is estimated having a 0% fill ratio,
- the substrate layer is the layer below the routing region.

1. Calculate the routing capacitance per unit length of a wire in each of the 4 routing layers under the above assumptions. In the solution, the geometrical design rules and electrical parameters from the design rules[1] are used. The relative permittivity of the inter-layer insulators is $\epsilon_r = 3.9$, except for the insulator between wires in the same layer, where $\epsilon_r = 4.1$.