Problem 15: Optimal Transistor Ratios

In N. Weste Section 4.6.1, the total delay t_{inv} through a pair of identical inverters is discussed. It is assumed that pull-up and pull-down transistor lengths are identical ($L = L_p = L_n$), whereas the ratio of the transistor widths is B ($B \equiv \frac{W_p}{W_n}$). It is proven, that t_{inv} assumes the same value for both $B = 1$ and $B = \frac{\mu_n}{\mu_p}$.

Determine the value of B, which yields the smallest value of t_{inv} for a given area.

Problem 16: Pass Transistor Circuit

Construct a pass-transistor circuit realizing the SUM function of an adder. The answer must include (a) a sketch illustrating the principle (multiplexor), (b) a transistor diagram and (c) a draft layout. The SUM function can be written

$$SUM = a \cdot b \cdot c + a \cdot \overline{b} \cdot \overline{c} + \overline{a} \cdot b \cdot \overline{c} + \overline{a} \cdot \overline{b} \cdot c$$

Problem 17: Domino CMOS Circuit

In Figure 1, the layouts of two different domino-CMOS circuits are shown. Both circuits realize the same function:

$$F = a \cdot (b + c + d + e + f)$$

In this problem, the charge redistribution properties of both circuits are discussed. All transistor geometries are $l = 0.18\mu m$ and $w = 0.28\mu m$. Geometrical design rules and electrical parameters should be taken from the design rules[1]. Finally, $V_{DD} = 1.8V$.

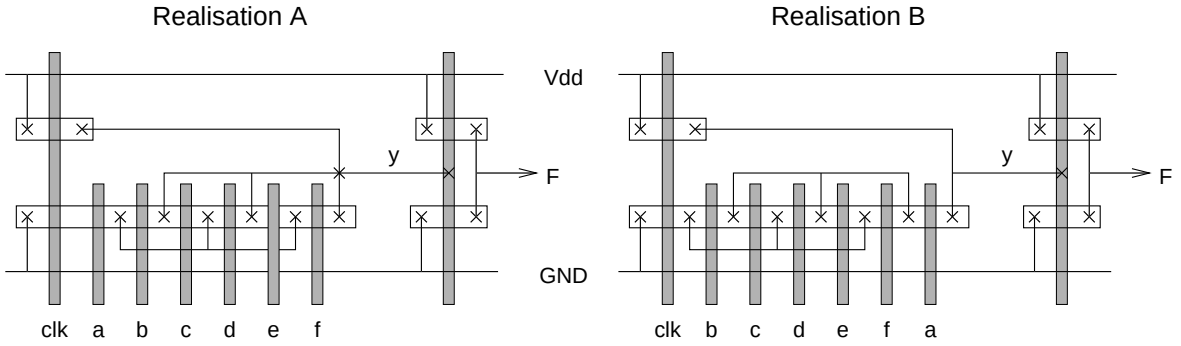

Figure 1: Domino circuits realizing $F = a \cdot (b + c + d + e + f)$

1. Draw the transistor diagrams corresponding to the layouts,
2. Calculate the gate thresholds V_{kip} for the inverters at the output of the circuit,
3. Describe the sequences of input signals (CLK, a, b, c, d, e, and f) causing the worst possible situations with respect to charge redistribution,
4. Calculate the voltages, to which the inverter inputs (y) are reduced due to charge redistribution,
5. What can you conclude from these investigations?
   Which conditions have been ignored in the analysis, and how may these conditions influence on the result?

Problem 18: Design of output buffer

Design an output buffer that will buffer an external load of 50pF in 5ns. The internal driver has W_p=W_n=0.5μm, L_p=L_n=0.25μm. V_{DD}=2.5V:

1. Calculate the current drawn by 16 such buffers that are simultaneously driven at a clock rate of 100 MHz
2. Determine the number of power and ground pads necessary for the 16 buffers, when the length of the V_{DD} and V_{SS} to each pad is 120μm

Problem 19: Power dissipation

Calculate the approximate dynamic and short-circuit power dissipated in a chip operating with a V_{DD} of 1.8V at 450MHz with an internal switched capacitance of 300pF, assuming that the average rise/fall time is 25ps.
Calculate the approximate dynamic and short-circuit power dissipated in the same chip, when V_{DD} is 1.2V Determine the short-circuit dissipation change when the average rise/fall time is 150ps.