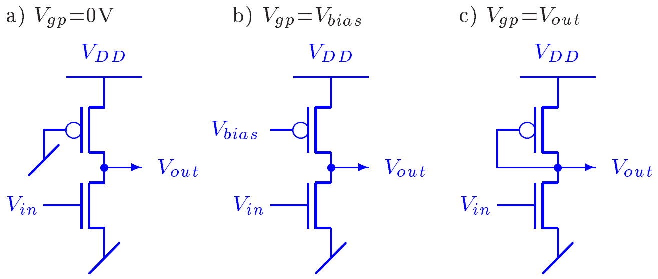
Problem 7: Backbias Effect

Sometimes the substrate is connected to a voltage called the substrate bias to alter the treshold of the n-transistors. If the treshold of an n-transistor is to be raised, explain to what polarity the voltage would be connected.
Draw a circuit diagram showing V_{DD}, V_{SS}, and substrate supplies connected to an inverter.

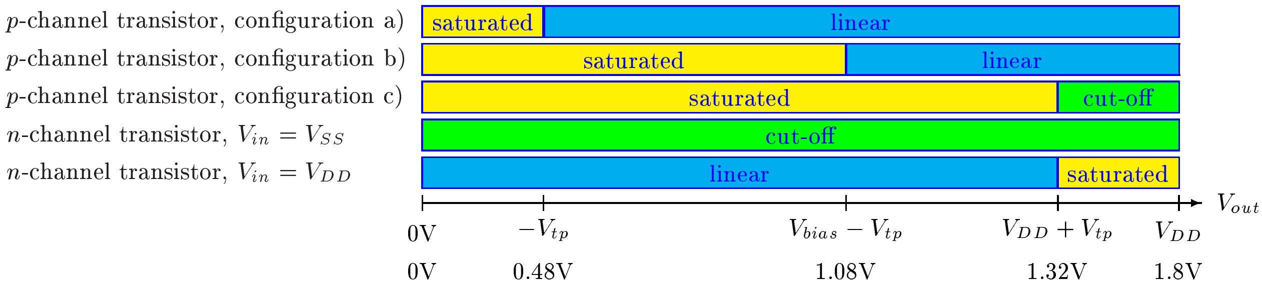
Problem 8: Current Source

Under what voltage conditions is a p-transistor with a source connected to V_{DD}=1.8V (V_{tp}=-0.48V) a good current source?

Problem 9: Logic Configurations



1.a: Pseudo-nMOS NOR gate



1.b: CMOS NOR gate configurations

In Figure 1.a, various *pseudo-nMOS* configurations of a NOR gate is shown. Such a NOR gate may be found in ROM or RAM address decoding or realisations of PLA's. Typically, the gate of the p-channel transistor is connected as shown. However, a bias voltage, ($0V < V_{bias} < V_{DD}$), may be used as well (see N. Weste Section 5.4.3). Finally, $V_{gp} = V_{out}$ may be used.

The configurations are analysed using the equivalents shown in Figure 1.b. V_{dd}=1.8V, V_{bias}=0.6V and l_n=l_p=0.18μm, w_n=w_p=0.28μm. In addition, minimum geometries as given in the design rules sheet[1] should be used.

a. For each configuration, specify the working ranges (cut-off, linear and saturated) for both n- and p-channel transistors (in terms of V_t, V_{DD}, V_{bias}, and V_{out}).

b. Determine the output high voltage, V_{outH}, and the output low voltage, V_{outL}, for each configuration[2].

[1] *Design Rules and Electrical Parameters for a 0.18 micron CMOS Process*
[2] Hint: Write down the equations for $-I_{dsp} = I_{dsn}$ and determine V_{out}. Remember, that $I_{dsp} = -\beta_p((V_{gs} \ldots$

Problem 10: Layout and Transistor Diagrams

a. Draw the masks for 1) a p-channel transistor, 2) a n-channel transistor, and 3) two transistors, in which the gate of one transistor is connected to the drain of the other transistor through a metal-1 wire[3].

b. Draw the transistor diagrams, draft layouts and mask layouts for 1) a 2-input NOR-gate and 2) a 4-input NOR gate. The layout should be drawn in such a way, that it may be generalised for an arbitrary number of inputs[3].

c. Draw a transistor diagram, draft layout and mask layout for a 2-input CMOS multiplexor[3]. It is assumed that the control signals are available in both true and complemented form[4].

Problem 11: Transistor Capacitances in Saturation

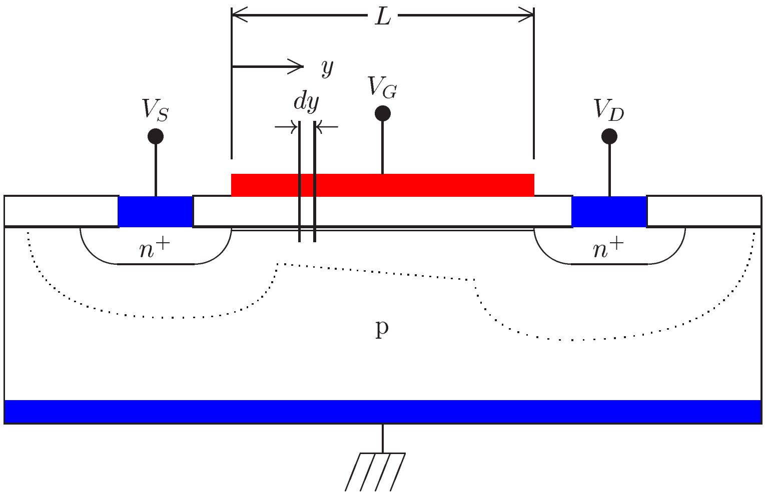


Figure 2: 'Idealized' cross section of an n-channel MOS transistor

a. Show that the capacitance C_{gs} (see Figure 2) between gate and source and the capacitance C_{gd} between gate and drain with an approximation is given by

$$C_{gs} \simeq \frac{2}{3} W\ L\ C_{ox} \qquad\qquad C_{ds} \simeq 0$$

when the transistor operates in saturation[5].

b. Determine the ratio τ_{tr} between the total electron charge, Q_{CTOT}, and the drain current, I_{DS}, in saturation:

$$\begin{aligned}(Q_{CTOT} &= \int_0^L \int_0^W Q_C dz dy) \\ \tau_{tr} &= -\frac{Q_{CTOT}}{I_{DS}}\end{aligned}$$

[3] In the reply, transistors with $(W, L) = (0.28\mu m; 0.18\mu m)$ are used. In addition, minimum geometries as given in the design rules sheet[1] should be used

[4] Hint: see the answers to Problem 4

[5] Hint! Determine the potential distribution along the channel, $V(y)$, by writing down an expression for the differential voltage drop dV over a small section of the channel, dy. The mobile inversion charge Q_C in the channel is given by

$$Q_C(y) \simeq -C_o\,(V_{gs} - V_T - V(y))$$