Problem 1

Question 1.1

The operation of the dynamic latch can be summarized as follows:

$\phi = 0$: The latch holds its previous state.
If Q is low, this value is held capacitively, as the feedback through P2 prevents X to become low.
Q high may be held actively high, if X is low, or capacitively high, if X is high.

$\phi = 1$: The latch is transparent.
When Q is high, P2 is off, and the value on D will propagate through X to Q. A falling transition on Q will be positively fed back to X through P2.
If Q is low, P2 is on holding X high. A low value on D supports this, whereas D high will pull X low through N1-N2. The shift will take place, if and only if, the voltage V_X drops below the gate threshold of N3-N4-P3. In this case, the positive feedback through P2 will fulfill the shift.

The equivalent diagram depicts the above requirement. If β_{N1-N2} is high enough, the shift will take place. As V_X is falling, the conductance of P2 increases, while the conductance of N1-N2 falls, until V_X reaches V_{kip}.

N4 is biased by V_{DD}, thus much more conductive than P3 and N3 at the shift. Therefore, N4 does not affect the calculation of V_{kip}:

$$\frac{\beta_n}{\beta_p} = \frac{KP_n}{KP_p}\frac{W_n}{W_p}\frac{L_p}{L_n} = \frac{263}{60}\frac{0.5\mu m}{0.5\mu m}\frac{0.25\mu m}{0.25\mu m} = 2.09^2 \quad (1)$$

$$V_{kip} = \frac{V_{DD} + V_{tp} + V_{tn}\cdot\sqrt{\frac{\beta_n}{\beta_p}}}{1+\sqrt{\frac{\beta_n}{\beta_p}}} = \frac{3.0 - 0.55 + 0.56\cdot\sqrt{\frac{\beta_n}{\beta_p}}}{1+\sqrt{\frac{\beta_n}{\beta_p}}} = \underline{\underline{1.17V}} \quad (2)$$

Question 1.2

When body effects are disregarded, N1-N2 is replaced by a single transistor $2\times 0.25\mu m$ long. At the minimum length of P2, V_X is at V_{kip}, and both P2 and N1-N2 operate in the linear region:

$$\beta_n(V_{DD} - V_{tn} - \frac{1}{2}V_{kip})V_{kip} = \beta_p(V_{DD} + V_{tp} - \frac{1}{2}(V_{DD} - V_{kip}))(V_{DD} - V_{kip}) \quad (3)$$

$$\frac{\beta_n}{\beta_p} = \frac{KP_n}{KP_p}\frac{W_n}{W_p}\frac{L_p}{L_n} \Leftrightarrow L_{P2,min} = \frac{KP_p}{KP_n}\left.\frac{\beta_n}{\beta_p}\right|_{R_n,max} L_n \quad (4)$$

$$L_{P2,min} = \frac{KP_p}{KP_n}\cdot L_n \frac{\frac{1}{2}V_{DD} + V_{tp} + \frac{1}{2}V_{kip}}{V_{DD} - V_{tn} - \frac{1}{2}V_{kip}}\frac{V_{DD} - V_{kip}}{V_{kip}} \quad (5)$$

$$= \frac{60}{263}(2\cdot 0.25\mu m)\frac{1.54}{1.85}\frac{1.82}{1.17} = 0.15\mu m \quad (6)$$

Thus, choosing the minimum channel length from the design rules suffices:

$$L_{P2} = \underline{\underline{0.25\mu m}} \quad (7)$$

 ... continued on the next page

Problem 3

Question 3.1

The total power dissipated, P, is

$$P = P_{\rm S} + P_{\rm d} + P_{\rm SC}$$

The static power dissipation, P_S, for CMOS complementary logic is due to 'diode' leakage currents between $^{a)}$ n-type diffusions and substrate, I_n, $^{b)}$ p-type diffusions and n-well regions, I_p, and $^{c)}$ n-well regions and substrate, I_w. An upper limit on P_S can be obtained assuming that half the number of pn-junctions are unbiased, the other half reverse biased by V_{DD}:

$$\begin{aligned}
I_n &= [\text{ total area of } n\text{-type diffusions }] \cdot JS_n && (19)\\
&= [\ 40000 \cdot (0.5 \times 0.75\mu m^2)\ ] \cdot 30nA/m^2 \ = \ 0.45fA\\
I_p &= [\text{ total area of } p\text{-type diffusions }] \cdot JS_p && (20)\\
&= [\ 40000 \cdot (0.5 \times 0.75\mu m^2)\ ] \cdot 40nA/m^2 \ = \ 0.60fA\\
I_w &= [\text{ total area of } n\text{-well regions }] \cdot JS_w && (21)\\
&= [\ \frac{1}{2} \cdot (1 \times 1mm^2)\ ] \cdot 1.0nA/m^2 \ = \ 0.50fA\\
P_{\rm S} &= V_{dd} \cdot (\ I_n + I_p + I_w\ ) \ = \ 1V \cdot (\ 0.45 + 0.60 + 0.50\ )fA \ = \ 1.55fW && (22)
\end{aligned}$$

Thus, the static power consumption will be negligible.

The dynamic power dissipation, P_d, accounts for the charging and discharging of the internal load capacitance, C_L. The load capacitance consists of routing capacitance, $C_{L,r}$, gate capacitances, $C_{L,g}$, and diffusion capacitances, $C_{L,d}$:

$$\begin{aligned}
C_{L,r} &= [\text{ area Metal1 }] \cdot C_{m1} + [\text{ area Metal2 }] \cdot C_{m2} + [\text{ area Metal3 }] \cdot C_{m3} && (23)\\
&= 1mm^2 \cdot (\ 9\% \cdot 23.9 + 6\% \cdot 11.5 + 3\% \cdot 7.4\ )pF/mm^2 \ = \ 3.1pF\\
C_{L,g} &= 40000 \cdot (W_n + W_p) \cdot L \cdot C_{ox} \ = \ 40000 \cdot 1 \cdot 0.25 \cdot 6.9fF \ = \ 69pF && (24)\\
C_{L,d} &= area_n \cdot C_{jna} + area_p \cdot C_{jpa} + perimeter_n \cdot C_{jnp} + perimeter_p \cdot C_{jpp} && (25)\\
&= 40000 \cdot [\ 0.5 \cdot 0.75 \cdot (596 + 690) + 2 \cdot (0.5 + 0.75) \cdot (122 + 138)]aF\\
&= 45pF\\
C_L &= C_{L,r} + C_{L,g} + C_{L,d} \ = \ (3.1 + 69 + 45)pF \ = \ 117pF && (26)\\
P_{\rm d} &= A \cdot C_L \cdot V_{dd}^2 \cdot f \ = \ 20\% \cdot 117pF \cdot 1V^2 \cdot 100MHz \ = \ 2.4mW && (27)
\end{aligned}$$

The short-circuit power dissipation, P_{SC}, is zero, as $V_{DD} \leq V_{tn} - V_{tp}$. At no time during the shift can a path exist between the positive and negative supplies, no matter the time delays during the shift.

The total power dissipation is

$$P \ = \ P_{\rm S} + P_{\rm d} + P_{\rm SC} \ \approx \ P_{\rm d} \ = \ \underline{\underline{2.4mW}} \qquad (28)$$

As long as V_{DD} remains above V_{tn} and well below $V_{tn} - V_{tp}$, the power dissipation is proportional to V_{DD}^2. Close to the upper limit, substantial subthreshold currents will increase the power dissipation.

 ... continued on the next page