TECHNICAL UNIVERSITY OF DENMARK
(M.Sc.Eng.-course)

Written test on 13th December 1999

Course: Design of Integrated Circuits 1 Course no. 49260

Permitted aids: Any

Weighting: All questions are weighted equally.

A 0.25μm process is used in all problems. Geometrical design rules, list of symbols used as well as electrical parameters for the process is found in Appendix 1 on Page 5. The parameters in Appendix 1 should be used, unless the text specifies otherwise.

Problem 1

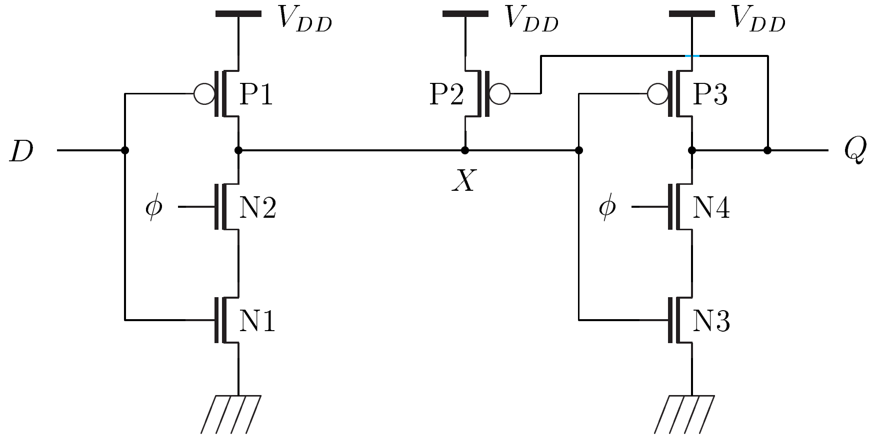

Figure 1.a: Transistor diagram of single clock latch

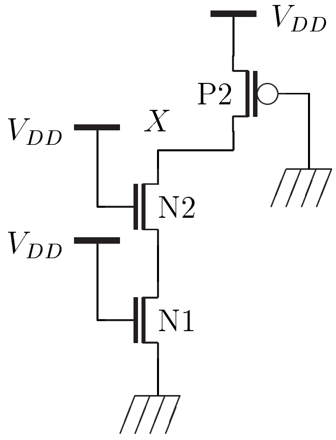

Figure 1.b: Equivalent diagram

In this problem, the design of the dynamic single clock latch shown in Figure 1.a is discussed. The P2 transistor is introduced to make the latch less susceptible to noise and leakage currents. However, for correct operation, it is necessary to dimension the sizes of the transistors properly.
The channel width of any transistor is 0.5μm. The minimum channel length is used for all transistors, except for transistor $P2$. The supply voltage is $V_{DD} = 3V$. In the reply, body effects are disregarded.

Question 1.1

Discuss, which matters must be considered in the design of transistor $P2$. Motivate why this analysis can be simplified to the equivalent shown in Figure 1.b, where $V_X = V_{kip}$, the gate treshold of the stage N3-N4-P3.
Calculate V_{kip}.

Question 1.2

Use the equivalent diagram in Figure 1.b to determine the length of transistor $P2$ such that the latch can shift from high to low state.

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Problem 3

This problem considers the estimation of power dissipation for a digital logic block, part of an integrated circuit under design. The IC will be operated at low supply voltage, $V_{DD} = 1V$.
The logic block is designed using conventional CMOS complementary logic. The complexity of the block is equivalent to 40000 inverters, i.e. it is assumed that the circuit consists of 40000 inverters. The clock frequency of the circuit, f, is $100MHz$. The nodal activity, A, is 20%, i.e. in each clock cycle 20% of the internal nodes change state. The average rise and fall times, t_{dr} and t_{df}, are $300ps$.
The logic block is allocated a design window of $1mm \cdot 1mm$. In this design window, half the area is assumed to be a n-well region. The routing capacitance is estimated by the assumption that internal signals are routed (and thus loaded) in metal over substrate

- by a $Metal1$ area of 9% of the design window,
- by a $Metal2$ area of 6% of the design window, and
- by a $Metal3$ area of 3% of the design window.

The perimeter contributions of the metal areas are disregarded.
Each of the above mentioned 40000 inverters is assumed to have the following properties:

- the channel width, W, and length, L, are $(W, L) = (0.50\mu m, 0.25\mu m)$,
- the size of any diffusion region is $(W_d, L_d) = (0.50\mu m, 0.75\mu m)$.

The following parameters describing the typical leakage currents are provided for the process:

- the reverse bias saturation current between n-type diffusions and substrate:

$$JS_n = 30nA/m^2$$

- the reverse bias saturation current between p-type diffusions and n-well:

$$JS_p = 40nA/m^2$$

- the reverse bias saturation current between n-well regions and substrate:

$$JS_w = 1.0nA/m^2$$

Question 3.1

Calculate the total power dissipation of the logic block under consideration using the assumptions above.
Discuss the consequences of modifying the supply voltage, V_{DD}.

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Appendix 1: 0.25μm CMOS process parameters and design rules

Transistor parameters		
Current factor $[\mu A/V^2]$	KP_n	263
	KP_p	60
Threshold voltage $[V]$	V_{tn0}	0.56
	V_{tp0}	- 0.55
Body effect coefficient $[\sqrt{V}]$	γ_n	0.336
	γ_p	0.695
Bulk potential $[V]$	ϕ_{bn}	0.323
	ϕ_{bp}	- 0.323
Channel length modulation $[V^{-1}]$	λ_n	0.010
	λ_p	0.046

Film thickness		
Gate oxide thickness	t_{ox}	50 Å
Field oxide thickness	t_F	3500 Å
Oxide thickness between poly and metal-1	t_{mp}	8000 Å
Oxide thickness between metal-1 and metal-2	t_{mm}	9000 Å
Thickness of polysilicon layer	t_p	2000 Å
Thickness of metal-1 and metal-2 layers	t_{m1}	6200 Å

Capacitances					
		Area $aF/\mu m^2$		Perimeter $aF/\mu m$	
metal-3	to substrate	C_{m3}	7.4	C_{m3p}	30
metal-2	to substrate	C_{m2}	11.5	C_{m2p}	34
metal-1	to substrate	C_{m1}	23.9	C_{m1p}	40
poly (over field oxide)	to substrate	C_p	88.6	C_{pp}	42
n^+ diffusion (0V)	to substrate	C_{jna}	690	C_{jnp}	138
p^+ diffusion (0V)	to substrate	C_{jpa}	596	C_{jpp}	122
gate capacitance		C_{ox}	6900	—	

In the diagram below, an excerpt of the geometrical design rules are shown. All sizes given are minimum sizes, except for contacts and metal vias, which are only sizes.