# Problem 3

## Question 3.1

The transistor diagram illustrates an NP CMOS $\phi$ logic stage. The pipeline consisting of a n-logic block, a p-logic block and finally, a $C^2$MOS latch. During $\phi = 0$, nodes $x3$ and $x4$ are precharged to 1 and 0, respectively, while the output latch stores the previous state. When $\phi = 1$, both logic blocks evaluate, and the output latch is transparent.
The function realized by the transistor network is

$$f = \begin{cases} f^*, & \phi = 0 \\ ((\, \overline{a} + \overline{b}\,) \cdot \overline{c} + d\,) \cdot e, & \phi = 1 \end{cases} \tag{14}$$

where $f^*$ denotes the previous value of $f$.
The evaluation proceeds by conditional discharging of the outputs of the logic blocks. Each logic block can make at most one transition, $x3$ from 1 to 0, $x4$ from 0 to 1. The inputs to the n-logic block are allowed to transition from 0 to 1, while the inputs to the p-logic block may transition from 1 to 0. It is evident that the internal node, $x3$, satisfies the above requirement.

## Question 3.2

The capacitances of the nodes are composed by combinations of the following capacitances:

| | 'area' $[\mu m^2]$ | 'perimeter' $[\mu m]$ | n-type $[fF]$ | p-type $[fF]$ |
|---|---|---|---|---|
| end diffusion | $2.75 \cdot 2.5$ | $2 \cdot (2.75 + 2.5)$ | $C_{n1} = 8.21$ | $C_{p1} = 13.5$ |
| internal diff with contact | $3.0 \cdot 2.5$ | $2 \cdot (3.0 + 2.5)$ | $C_{n2} = 8.72$ | $C_{p2} = 14.3$ |
| internal diff, no contact | $1.5 \cdot 2.5$ | $2 \cdot (1.5 + 2.5)$ | $C_{n3} = 5.65$ | $C_{p3} = 9.33$ |
| gate capacitance | $1.0 \cdot 2.5$ | - | $C_g = 4.88$ | |
| metal-1 wire | $1.5 \cdot 20$ | $2 \cdot 20$ | $C_{m1} = 2.71$ | |
| metal-2 wire | $1.5 \cdot 30$ | $2 \cdot 30$ | $C_{m2} = 3.89$ | |

**Node $y1$:** $$C_{y1} = C_{n1} + C_{n2} + C_{m1} = \underline{\underline{19.6fF}} \tag{15}$$

**Nodes $z2$ and $z7$:** $$C_{z2} = C_{z7} = C_{n3} = \underline{\underline{5.65fF}} \tag{16}$$

**Node $x3$:** $$C_{x3} = C_{p1} + C_{n2} + C_g + 2C_{m1} = \underline{\underline{32.5fF}} \tag{17}$$

**Node $x4$:** $$C_{x4} = C_{n1} + C_{p2} + 2C_g + 3C_{m1} = \underline{\underline{40.4fF}} \tag{18}$$

**Nodes $z5$ and $z8$:** $$C_{z5} = C_{z8} = C_{p3} = \underline{\underline{9.33fF}} \tag{19}$$

**Node $y6$:** $$C_{y6} = C_{p1} + C_{p2} + C_{m1} = \underline{\underline{30.5fF}} \tag{20}$$

**Node $f$:** $$C_f = C_{n1} + C_{p1} + C_{m1} + C_{m2} = \underline{\underline{28.3fF}} \tag{21}$$

The effective resistances of the transistors:

$$R_n = R_{n,\Box} \cdot \frac{L}{W} = \frac{\frac{L}{W}}{KP_n \cdot (V_{DD} - V_{tn0})} = \frac{1}{98\mu \cdot (3 - 0.8)} \frac{1}{2.5}\Omega = \underline{\underline{1.86k\Omega}} \tag{22}$$

$$R_p = R_{p,\Box} \cdot \frac{L}{W} = \frac{\frac{L}{W}}{KP_p \cdot (V_{DD} + V_{tp0})} = \frac{1}{38\mu \cdot (3 - 0.8)} \frac{1}{2.5}\Omega = \underline{\underline{4.79k\Omega}} \tag{23}$$

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**Question 3.3**

During precharge, the internal node $x4$ is discharged to 0V. The worst-case shift $f_{0\to 1}$ occurs for any set of inputs, which discharge $f$ to 0 during one clock cycle and charges $f$ to 1 in the following clock cycle, $(\overline{f}, f)$.
The RC-model of the shift is shown in Figure 3.a. Using the Penfield-Rubinstein model, the RC equivalents yields

$$\begin{aligned} t_{dr} &\approx R_p \cdot (\ 2 \cdot (C_{z7} + C_f) + C_{z8}\ ) \\ &= 4.79 \cdot (\ 2 \cdot (5.65 + 28.3) + 9.33\ )\text{ps} \ = \ \underline{\underline{370\text{ps}}} \end{aligned} \tag{24}$$

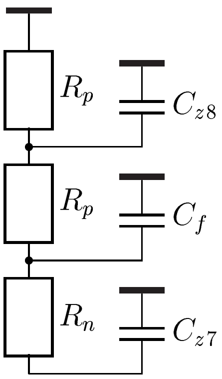


Figure 3.a: Calculation of $t_{dr}$

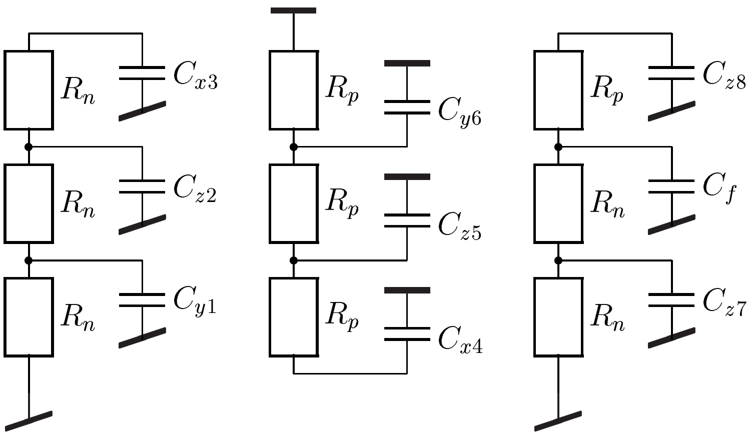


Figure 3.b: Calculation of $t_{df}$

Similarly, during precharge, the internal node $x3$ is charged to $V_{DD}$. The worst-case shift $f_{1\to 0}$ occurs, when the transition has to pass from the inputs over the pipelined blocks to the output, while charging and discharging the maximum capacitances over the narrowest string of transistors. This occurs for the input pattern $(abcde) = (11001)$ following any pattern that charges the output $f$.
According to definition, the worst-case delay is the sum of the delays of each logic block in the pipeline. The RC-model is shown in Figure 3.b and consists of 3 separate circuits, one for each block in the pipeline, for calculation of $t_{dn}$, $t_{dp}$, and $t_{dl}$:

$$t_{df} = t_{dn} + t_{dp} + t_{dl} \tag{25}$$

$$\begin{aligned} &\approx R_n \cdot (\ C_{y1} + 2 \cdot C_{z2} + 3 \cdot C_{x3}\ ) + R_p \cdot (\ C_{y6} + 2 \cdot C_{z5} + 3 \cdot C_{x4}\ ) + \\ &\quad R_n \cdot (\ C_{z7} + 2 \cdot (C_f + C_{z8})\ ) \end{aligned} \tag{26}$$

$$\begin{aligned} &= 1.86 \cdot (\ 19.6 + 2 \cdot 5.65 + 3 \cdot 32.5\ ) + 4.79 \cdot (\ 30.5 + 2 \cdot 9.33 + 3 \cdot 40.4\ ) + \\ &\quad 1.86 \cdot (\ 5.65 + 2 \cdot (28.3 + 9.33)\ )\text{ps} \ = \ \underline{\underline{1.21\text{ns}}} \end{aligned} \tag{27}$$

In the calculation above, no correction is done to account for the fall and rise times of internal nodes $x3$ and $x4$. The Hedenstierna-Jeppson correction formulas can be used to further refine the calculation of $t_{df}$.

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