Problem 2

Question 2.1

When the latched value at the output is 0, the circuit is a ratioed design case. During evaluation, the circuit can fail, if the latched value of the output is low, and the output has to shift to high. In this case, if the resistance of the pull-down path, R_n, is too high compared to the resistance of $P2$, R_{P2}, the inverter can not shift.

To achieve proper operation, the resistance of $P2$ must be adequately high under all input combinations. This sets a lower limit on the length of $P2$. The worst case input corresponds to the maximum value of R_n, when the voltage at the inverter input is determined by voltage division (of V_{DD}) of $P2$ to $N10-N9-N8-N7-N2-N1$. If the voltage at the inverter input can go below the inverter threshold, V_{kip}, the inverter will shift. The necessary voltage to ensure a shift is lower, as positive feedback assists the shift from $V_{DD}+V_{Tp}$. In this analysis, the length of $P2$ is determined by the requirement that the inverter input drops below V_{kip}.

Furthermore, if the sources of the above n-channel transistors are precharged to V_{SS} rather than V_{DD}, the value of R_n is maximized. Thus, body effects help to achieve proper operation of the logic gate. Disregarding body effects will give the worst case situation corresponding to all sources precharged to V_{SS}.

The worst case input combination is

$$(\phi, ci, p_0, p_1, p_2, p_3, g_0, g_1, g_2, g_3) \quad = \quad \underline{\underline{(1,1,1,1,1,1,0,0,0,0)}} \qquad (8)$$

Question 2.2

The minimum value of L_{P2} is determined by the equivalent shown in Figure 1.a. At the minimum, the output of the logic network is at the inverter threshold, V_{kip}.

The inverter gate threshold is

$$V_{kip} \quad = \quad \frac{V_{DD}+V_{tp}+V_{tn}\sqrt{\frac{KP_n}{KP_p}}}{1+\sqrt{\frac{KP_n}{KP_p}}} \quad = \quad \frac{3.0-0.8+0.8\sqrt{\frac{98}{38}}}{1+\sqrt{\frac{98}{38}}}V \quad = \quad 1.34V \qquad (9)$$

At the minimum length of $P2$, the output is at V_{kip}, and both transistors operate in the linear region:

$$\beta_n(V_{DD}-V_{tn}-\frac{1}{2}V_{kip})V_{kip} \quad = \quad \beta_p(V_{DD}+V_{tp}-\frac{1}{2}(V_{DD}-V_{kip}))(V_{DD}-V_{kip}) \qquad (10)$$

$$\frac{\beta_n}{\beta_p} \quad = \quad \frac{KP_n}{KP_p}\frac{W_n}{W_p}\frac{L_p}{L_n} \quad \Leftrightarrow \quad L_{P2,min} \quad = \quad \frac{KP_p}{KP_n}\left.\frac{\beta_n}{\beta_p}\right|_{R_n,max} L_n \qquad (11)$$

$$L_{P2,min} \quad = \quad \frac{KP_p}{KP_n}\cdot L_n\,\frac{\frac{1}{2}V_{DD}+V_{tp}+\frac{1}{2}V_{kip}}{V_{DD}-V_{tn}-\frac{1}{2}V_{kip}}\,\frac{V_{DD}-V_{kip}}{V_{kip}} \qquad (12)$$

$$= \quad \frac{98}{38}\cdot 6.0\,\frac{1.37}{1.53}\,\frac{1.66}{1.34} \quad = \quad 2.6\mu m \qquad (13)$$

In the layout, $P2$ is chosen as $\underline{\underline{3.0\mu m}}$

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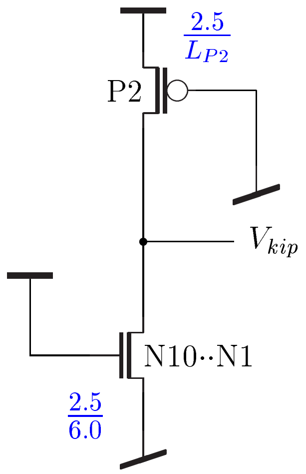

Figure 1.a: Equivalent diagram

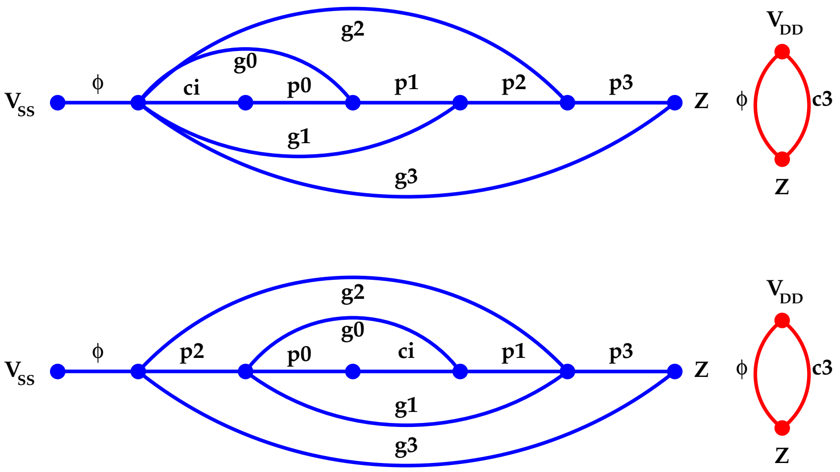

Figure 1.b: Pull-up and pull-down graphs

Question 2.3

The original as well as the modified pull-up and pull-down graphs are shown in Figure 1.b. The modified layout graph is used to create the single line-of-diffusion layout shown in Figure 2.

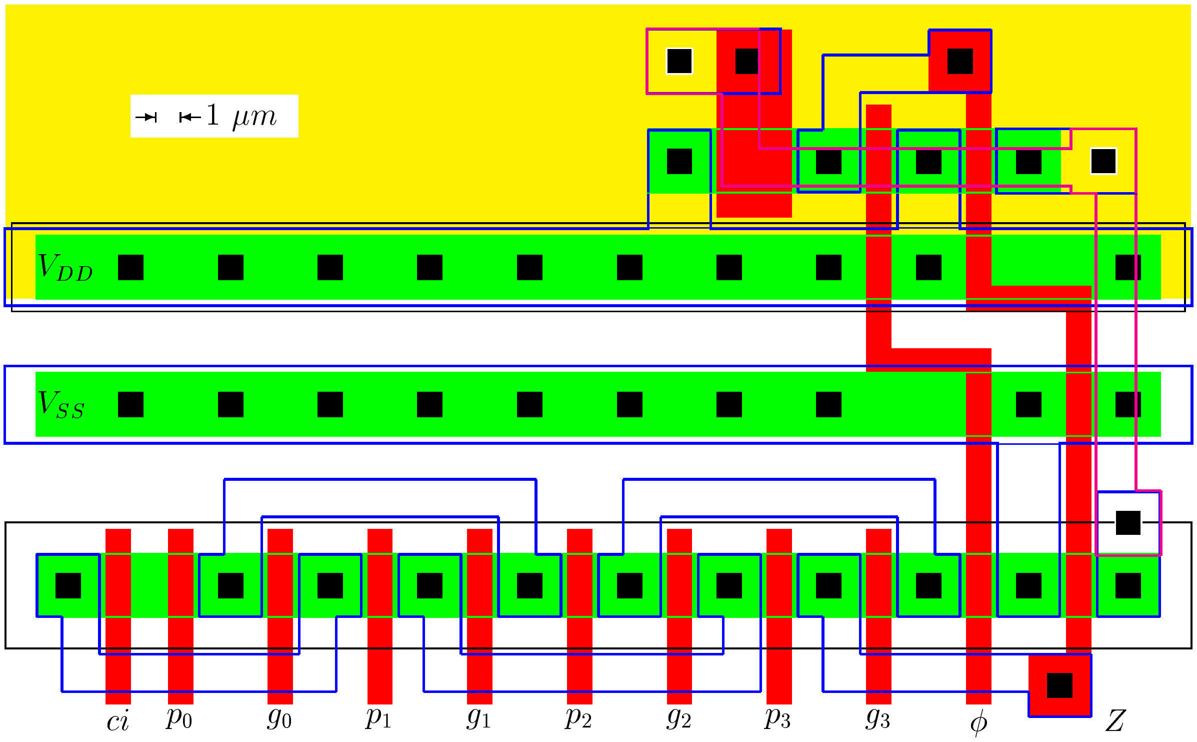

Figure 2: Single line-of-diffusion layout of the circuit