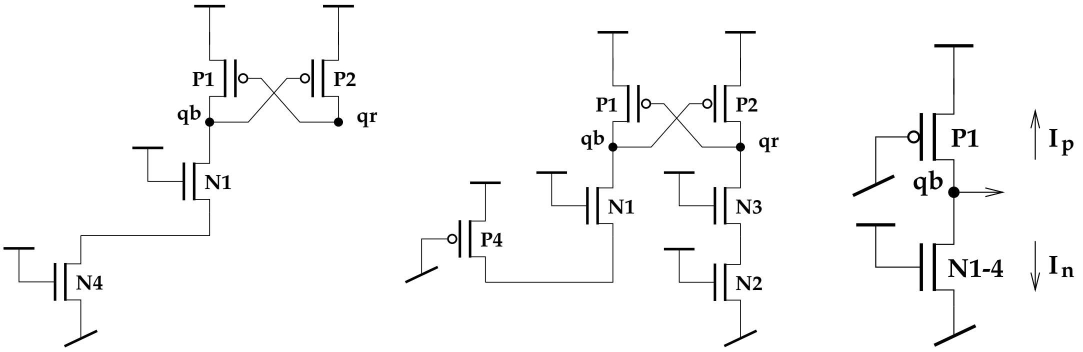
Problem 3

Question 3.1

At any point of time, only a single enable, EN_i, is active (high). When the enable signal of a pull-down stage is inactive, the stage is disconnected from nodes qb and qr. Thus, the analysis needs only to consider the Figure in the text, in which En_i is active, while all other stages are inactive.

P1-P2 realizes a differential pull-up stage with positive feedback similar to CVSL logic. N2-N3 forms a traditional pull-down stage for qr ($qr = \overline{En_i \cdot D_i}$), whereas N1-N4-P4 is a pull-down stage for qb ($qb = En_i \cdot D_i$) based on pass-transistor logic. Finally, P5-N5 is an inverting buffer for signal qr.



1.a: Mux with input $D_i = 0$ 1.b: Mux with input $D_i = 1$ 1.c: Equivalent

With $D_i = 0$, we find the situation shown in Figure 1.a. The left branch pulls down qb. Before the shift, $(qb, qr) = (1, 0)$. qr will not change, until qb is below $V_{DD} + V_{Tp}$. Correct static operation required ratioed design of P1 relative to N1-N4 to ensure, that qb can be pulled below this voltage. After this point, the positive feedback will complete the shift.

With $D_i = 1$, we find the situation shown in Figure 1.b. The right branch pulls down qr, while the left branch assists by pulling up qb. At low V_{DD}, the left branch may be inactive. Furthermore, N1 cannot pull qb above $V_{DD} - V_{Tn}$. The analysis is similar to the case when $D_i = 0$, and P2 must be ratioed relative to N2-N3.

The lowest, useful supply voltage, $V_{DD,min}$, is determined by the requirement, that all transistors are active. This requirement implies that $V_{DD,min}$ must contain a $V_{Tp,\text{worst-case}}$ and the 'ON' voltage of a conducting n-channel transistor, $V_{ds,n}[ON]$:

$$V_{DD,min} > V_{Tp,\text{worst-case}} + V_{ds,n}[ON]$$

Question 3.2

The equivalents are shown in Figures 1.b and 1.a. The worst-case situation is shown in Figure 1.a. The voltage on node qb is required to fall from V_{DD} to below $V_{DD} + V_{Tp}$. The voltage V_{qb} is determined by voltage division between P1 and the combined transistor N1-N4 (see Figure 1.c). The operating conditions are:

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N1-N4: $V_{gs,n} - V_{t,n} = V_{DD} - V_{t,n} > V_{DD} + V_{t,p} = V_{ds,n}$ (linear):

$$I_n = \beta_{N1-4}(V_{gs,n} - V_{t,n} - \frac{1}{2}V_{ds,n})V_{ds,n} = \beta_{N1-4}(V_{DD} - V_{t,n} - \frac{1}{2}V_{DD} - \frac{1}{2}V_{t,p})(V_{DD} + V_{t,p})$$

P1: $-(V_{gs,p} - V_{t,p}) = V_{DD} + V_{t,p} < -(V_{t,p}) = -V_{ds,p}$ (saturated):

$$I_p = \frac{1}{2}\beta_{P1}(V_{gs,p} - V_{t,p})^2 = \frac{1}{2}\beta_{P1}(V_{DD} + V_{t,p})^2$$

To pull qb below $V_{DD} + V_{Tp}$ requires that I_n is larger than I_p at this point:

$$\begin{aligned} I_n \geq I_p \quad &\Leftrightarrow \quad \frac{1}{2}\beta_{N1-4}(V_{DD} - 2V_{t,n} - V_{t,p})(V_{DD} + V_{t,p}) \geq \frac{1}{2}\beta_{P1}(V_{DD} + V_{t,p})^2 \\ &\Leftrightarrow \quad \beta_{N1-4}\frac{V_{DD} - 2V_{t,n} - V_{t,p}}{V_{DD} + V_{t,p}} \geq \beta_{P1} \end{aligned} \tag{3}$$

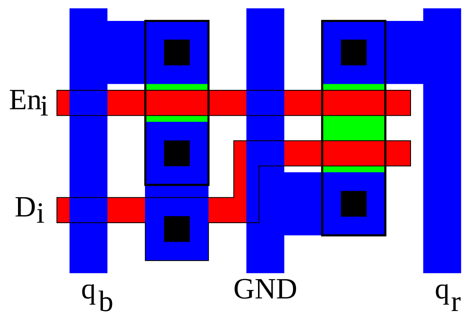
Inserting values and using the expression $\beta_x = KP_x \left(\frac{W}{L}\right)_x$ results in

$$\begin{aligned} KP_p \left(\frac{W}{L}\right)_1 &\leq \frac{1.0 - 2 \cdot 0.5 + 0.6}{1.0 - 0.6} \;\; KP_n \;\; \left(\frac{W}{L}\right)_{N1-4} \\ \Leftrightarrow \quad L_{P1} &\geq W_{P1} \;\; \frac{2}{3} \;\; \frac{38}{98} \;\; \frac{4}{5} = 0.52\mu m \end{aligned}$$

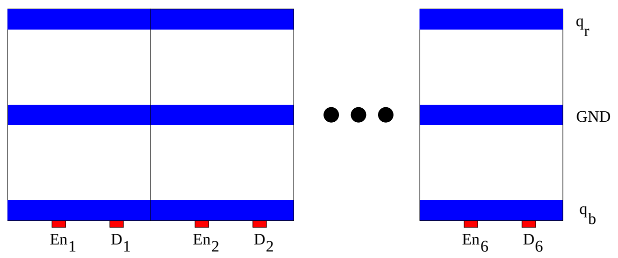
Thus, a minimum length transistor, $L_{P1} = 1\mu m$, will do the job.

Question 3.3

Many different layouts will solve the problem correctly. The mux has 6 identical pull-down segments, thus the effort should be concentrated on the pull-down segment. A layout of a pull-down segment and a draft layout of the entire multiplexor is shown below.



2.a: Layout of pull-down segment



2.b: Draft layout of mux

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