Problem 3

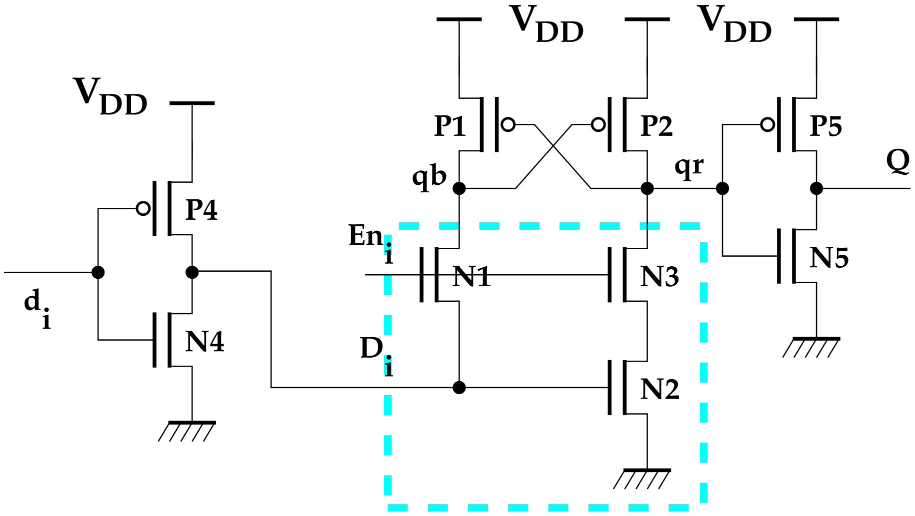

Figure 3: Transistor diagram of static multiplexor

Figure 3 shows a part of the transistor diagram of a static multiplexor realized in CMOS technology. The multiplexor is developed for use under low supply voltages, V_{DD}. The multiplexor consists of a common buffer/pull-up stage (transistors P1, P2, P5, and N5) and a number of identical pull-down stages (the figure inside the broken lines: transistors N1, N2 and N3). In the analysis, the signal D_i is assumed to be driven by an inverter (P4 and N4). Finally, exactly one enable signal, En_i, is assumed to be active at any moment. The geometries of N1, N2, N3, N4, N5, P4, and P5 are identical. Furthermore, the geometries of P1 and P2 are identical. $V_{DD} = 1.0V$, $V_{Tp} = -0.6V$ samt $V_{Tn} = +0.5V$.

Question 3.1

Explain, how the multiplexor works. Discuss which matters must be considered, when determining the sizes of the transistors to assure correct operation of the multiplexor at low supply voltages. Indicate the conditions, which determine the lowest useful supply voltage, $V_{DD,min}$.

Question 3.2

Draw an equivalent diagram for the shifts $D_i = V_{DD}$ and $D_i = 0$V, respectively. Determine the sizes of transistors P1 and P2, when

$$\left(\frac{W}{L}\right)_{N1} = \left(\frac{2.5\mu m}{1.0\mu m}\right) \quad \text{and} \quad W_{P1} = W_{P2} = 2.5\mu m$$

In the following question, a 6:1 multiplexor is considered consisting of 6 identical pull-down stages (the figure inside the broken lines: transistors N1, N2 and N3), P1 and P2 as well as P5 and N5.

Question 3.3

Draw a layout of the pull-down stage and illustrate, how the entire multiplexor is constructed.

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Appendix 1:
Process parameters and design rules for a 1.0μm CMOS process

Electrical parameters

Transistor parameters					
	n-channel		p-channel		Unit
Current factor	KP_n	98	KP_p	38	$\mu A/V^2$
Threshold voltage	V_{tn0}	0.8	V_{tp0}	- 0.8	V
Body effect coefficient	γ_n	0.52	γ_p	0.52	$\sqrt{V}$
Bulk potential	ϕ_{bn}	0.37	ϕ_{bp}	- 0.37	V
Channel length modulation	λ_n	0.01	λ_p	0.038	$1/V$

Capacitance (layer to substrate)				
	Area $fF/\mu m^2$		Perimeter $fF/\mu m$	
metal1	C_{m1}	0.032	C_{m1p}	0.052
poly	C_p	0.065	C_{pp}	0.062
n^+ diffusion (0V)	C_{jn}	0.39	C_{jnp}	0.50
p^+ diffusion (0V)	C_{jp}	0.60	C_{jpp}	0.85
gate capacitance	C_{ox}	1.7	—	

Sheet resistance		
Lag		$\Omega/\square$
metal1	R_{sm1}	0.06
poly	R_{sp}	33
n^+ diffusion	R_{sdn}	55
p^+ diffusion	R_{sdp}	70
n-well	R_{nw}	1250

Geometrical design rules