Problem 4

Question 4.1

Only a few, different capacitances are found in the symbolic layout. These are calculated below:

$$
\begin{aligned}
&\text{gate capacitance:} && \\
C_g &= W \cdot L \cdot C_{ox} = 1.0 \cdot 3.0 \cdot 1.7fF &&= 5.1fF \\
&\text{p-type end diffusion:} && \\
C_{pd} &= \text{` } area\,' \cdot C_{jp} + \text{` } perimeter\,' \cdot C_{jpp} && \\
&= 2.75 \cdot 3.0 \cdot 0.54fF + 2(2.75 + 3.0) \cdot 0.76fF &&= 13.2fF \\
&\text{n-type end diffusion:} && \\
C_{nd} &= 2.75 \cdot 3.0 \cdot 0.35fF + 2(2.75 + 3.0) \cdot 0.45fF &&= 8.1fF \\
&\text{n-type internal diffusion:} && \\
C_{ni} &= 3.0 \cdot 3.0 \cdot 0.35fF + 4(3.0) \cdot 0.45fF &&= 8.55fF \\
&\text{n-type diffusion on node z5:} && \\
C_{nu} &= 1.5 \cdot 3.0 \cdot 0.35fF + 2(1.5 + 3.0) \cdot 0.45fF &&= 5.62fF
\end{aligned}
$$

At this point, one may argue, that in an estimate, the difference between C_{nd} and C_{ni} is negligible. Furthermore, that contributions from metal and poly wires should be taken into consideration.
The required capacitances are

$$
\begin{aligned}
C_{z1} &= 2 \cdot C_g + C_{pd} + C_{ni} &&= 32.0fF \\
C_{z2} &= C_{nd} + C_{ni} &&= 16.7fF \\
C_{z3} &= C_{nd} + C_{ni} &&= 16.7fF \\
C_{z4} &= C_{nd} + C_{ni} &&= 16.7fF \\
C_{z5} &= C_{nu} &&= 5.6fF \\
C_{z6} &= 3 \cdot C_{ni} &&= 25.7fF
\end{aligned}
$$

Question 4.2

The circuit may fail during evaluation, if $z1$ due to charge sharing drops below the output inverter gate threshold, even though the pull-down network does not conduct. The worst case sequence must

a) discharge nodes $z2, z3, z4, z5$, and $z6$,

b) precharge $z1$ without precharging $z2, z3, z4, z5$, and $z6$,

c) evaluate connecting $z1$ to $z2, z3, z4$, and $z5$, but not to $z6$

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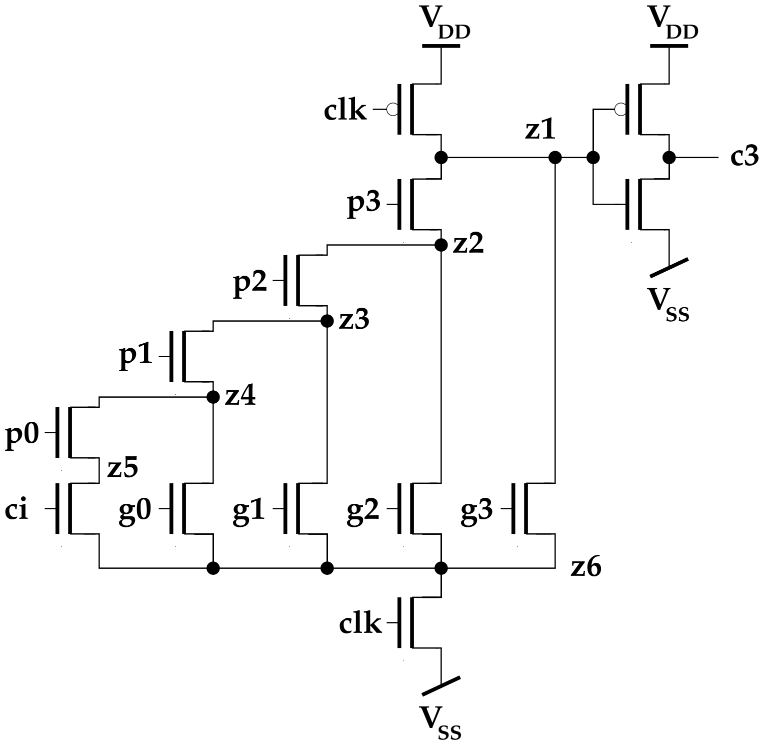

Several sequences may result in the worst case situation. In the Table below, the necessary conditions are listed (the first step may be realized in other ways):

vector	clk	ci	p0	p1	p2	p3	g0	g1	g2	g3
1	1	1	x	x	x	x	1	1	1	x
2	0	x	x	x	x	0	x	x	x	0
3	1	0	1	1	1	1	0	0	0	0

The voltage on node $z1$ is reduced to

$$V_{z1} \quad = \quad \frac{C_{z1}}{\sum_{i=1}^{5} C_{zi}} V_{DD} == \frac{32.0}{87.7} \cdot 5V = 1.82V$$

The output inverter gate threshold is

$$V_{kip} \quad = \quad \frac{V_{DD} + V_{tp} + V_{tn}\sqrt{\frac{KP_n}{KP_p}}}{1 + \sqrt{\frac{KP_n}{KP_p}}} = \frac{5.0 - 0.8 + 0.8\sqrt{\frac{98}{38}}}{1 + \sqrt{\frac{98}{38}}} V = 2.1V$$

The circuit will fail. This can be avoided by increasing the capacitance on node $z1$ and/or changing the output inverter gate threshold.