Problem 4

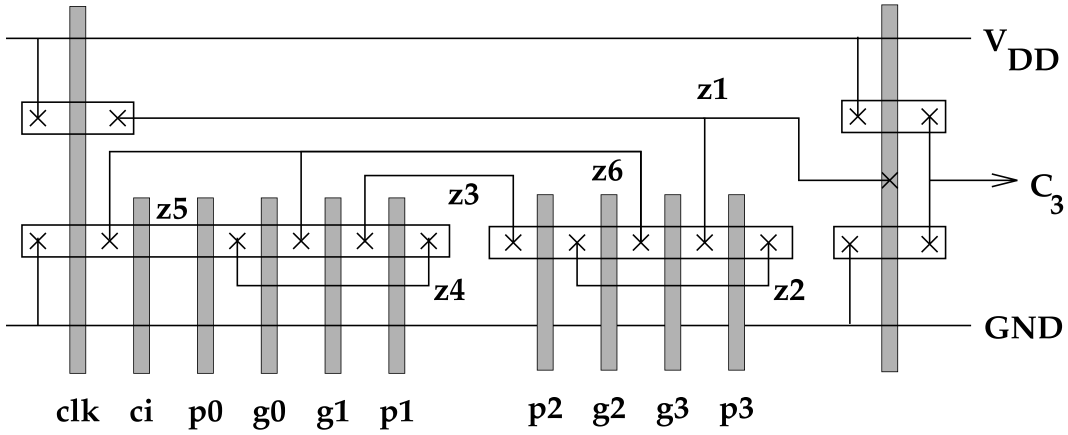

Figure 5: Domino CMOS circuit for calculation of carry

Figure 5 shows a symbolic layout of a circuit implementing carry C_3 of the Manchester *carry lookahead* adder. The transistor sizes are $L = 1\mu m$ and $W = 3\mu m$. $V_{DD} = 5V$.

Question 4.1

Calculate the capacitances of nodes $z1, z2, z3, z4, z5$, and $z6$, when minimal geometries are used. The capacitances of poly-wires over field oxide are not considered.

The output inverter gate threshold must be considered carefully during design to avoid, that the circuit fails during evaluation.

Question 4.2

Specify the sequence of input signals $(clk, ci, p0, p1, p2, p3, g0, g1, g2, g3)$, which results in the worst case with respect to charge sharing.
Determine the voltage, to which signal $z1$ is reduced due to charge sharing.
Compare this voltage to the gate threshold of the inverter at the output.

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Appendix 1:
Process parameters and design rules for a 1.0μm CMOS process

Electrical parameters

Transistor parameters					
	n-channel		p-channel		Unit
Current factor	KP_n	98	KP_p	38	$\mu A/V^2$
Threshold voltage	V_{tn0}	0.8	V_{tp0}	- 0.8	V
Body effect coefficient	γ_n	0.52	γ_p	0.52	$\sqrt{V}$
Bulk potential	ϕ_{bn}	0.37	ϕ_{bp}	- 0.37	V
Channel length modulation	λ_n	0.01	λ_p	0.038	$1/V$

Capacitance (layer to substrate)				
	Area $fF/\mu m^2$		Perimeter $fF/\mu m$	
metal1	C_{m1}	0.029	C_{m1p}	0.046
poly	C_p	0.058	C_{pp}	0.055
n$^+$ diffusion (0V)	C_{jn}	0.35	C_{jnp}	0.45
p$^+$ diffusion (0V)	C_{jp}	0.54	C_{jpp}	0.76
gate capacitance	C_{ox}	1.7	—	

Sheet resistance		
Lag		$\Omega/\square$
metal1	R_{sm1}	0.06
poly	R_{sp}	33
n$^+$ diffusion	R_{sdn}	55
p$^+$ diffusion	R_{sdp}	70
n-well	R_{nw}	1250

Geometrical design rules