Problem 1

Question 1.1

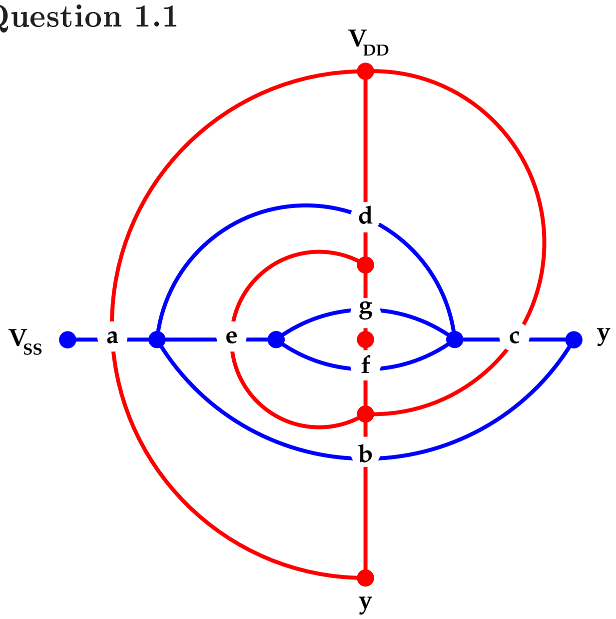

Figure 1.a: Pull-up and pull-down graphs

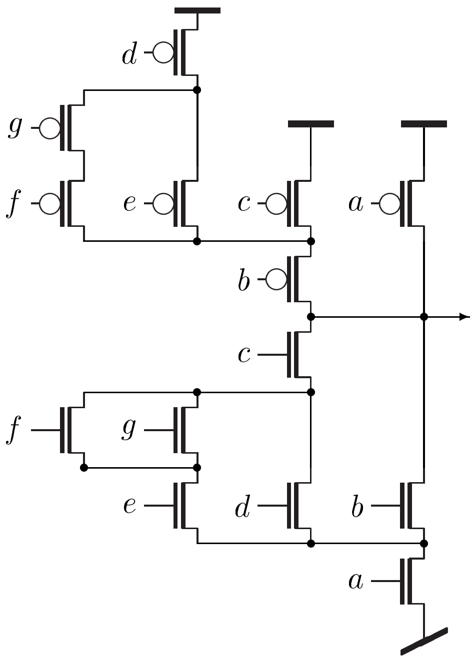

Figure 1.b: Equivalent diagram

Question 1.2

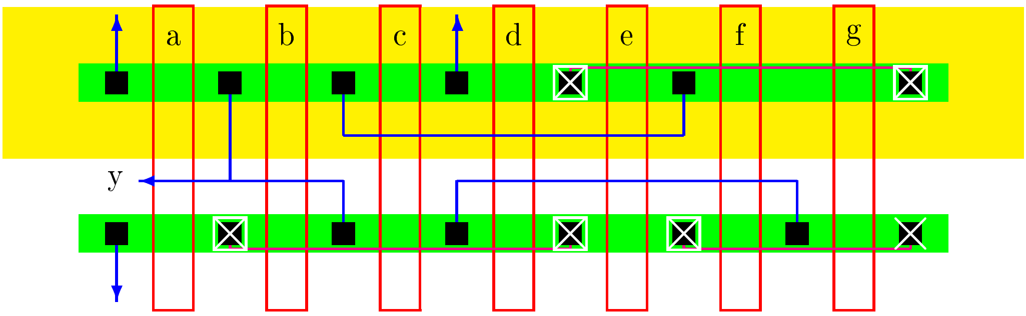

Figure 2: Draft layout of the circuit

A line-of-diffusion layout is drafted in Figure 2 based on the common euler path $abcdefg$. Minimum size diffusion lines yield the horizontal dimension of the boundary box $(2 \cdot 0.65 + 7 \cdot 0.25 + 6 \cdot 0.8)\mu m = 7.80\mu m$ not including n-well caps.
The vertical dimension must accomodate both transistor layer and routing requirements. The transistor rules gives a lower limit of $2.3\mu m$ (poly gate caps, diffusion widths and n-to-p distance). From the draft, two metal-1 route tracks must be placed between the diffusion lines, while metal-2 is used for additional routing. From this, the vertical dimension becomes $0.8\mu m$ larger.
Thus, the dimensions of the surrounding boundary box are $7.80\mu m \times 3.1\mu m$.

Problem 2

Question 2.1

The transistor diagram illustrates an NP CMOS ϕ logic stage. The stage consists of two n-logic blocks cascaded by a single p-logic block and a C^{2}MOS latch at the output. During $\phi = 0$, nodes qa and qd are precharged to 1, node qi is precharged to 0, and the output latch stores. When $\phi = 1$, the logic blocks evaluate, and the output latch is transparent. The function realized by both transistor networks is

$$f \;=\; \overline{f^{\times}} \;=\; \begin{cases} f^{*}, & \phi = 0 \\ \overline{(\,a \cdot b \cdot c \cdot d\,)}, & \phi = 1 \end{cases} \tag{1}$$

where f^{*} denotes the previous value of f or $f^{\times}$.
The inputs change while the circuits precharge. During evaluation, the inputs are allowed to make a rising transition, only, in any of the two realizations shown.

Question 2.2

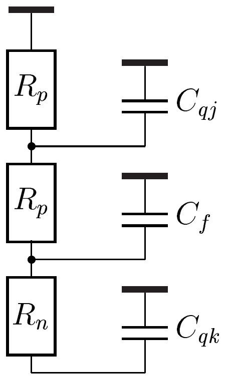

Figure 3.a: $t_{dr}(f)$

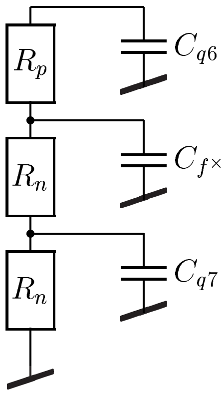

Figure 3.b: $t_{df}(f^{\times})$

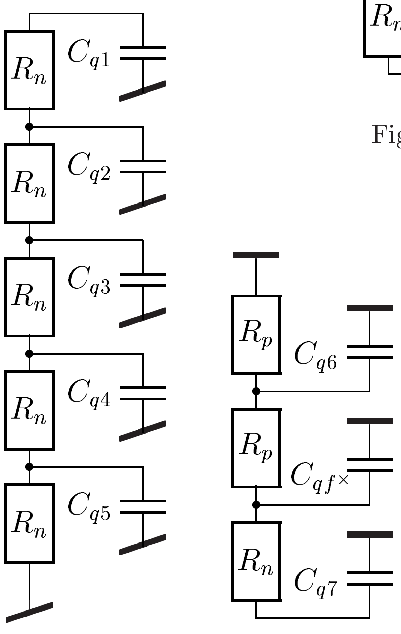

Figure 3.c: $t_{dr}(f^{\times})$

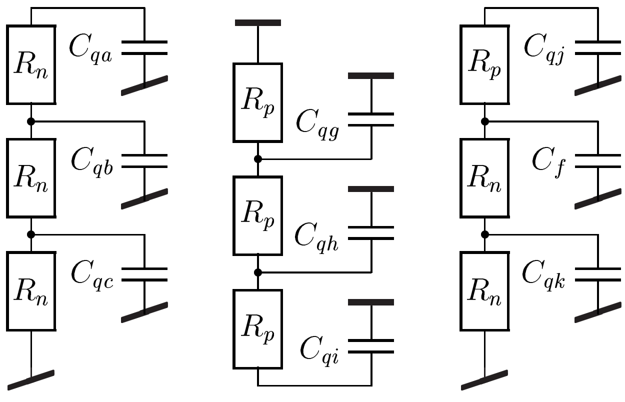

Figure 3.d: $t_{df}(f)$

By definition, rise and fall delays are additive. No corrections are made to account for the limited fall and rise times of internal signals (e.g. the Hedenstierna-Jeppson correction formulas).

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Most internal capacitances are readily located in the design rules. The metal-1 to metal-2 capacitance per unit area is estimated using:

$$C_{mm} = \frac{\epsilon_r \cdot \epsilon_0}{t_{mm}} = \frac{3.9 \cdot 8.85 pF/m^2}{9000} = 38.4 aF/\mu m^2 \qquad (2)$$

The data available in the design rules sheet does not allow for a useful estimate of the metal-1 to metal-2 perimeter capacitance. Depending on the actual design, this will introduce an underestimate of 50-600% of the metal-1 to metal-2 capacitance. Using this, the internal capacitances are calculated:

	'area' $[\mu m^2]$	'perimeter' $[\mu m]$	n-type $[aF]$	p-type $[aF]$
end diffusion	$0.65 \cdot 0.5$	$2 \cdot (0.65 + 0.5)$	$C_{n1} =$ 542	$C_{p1} =$ 474
internal (no contact)	$0.45 \cdot 0.5$	$2 \cdot (0.45 + 0.5)$	$C_{n3} =$ 417	$C_{p3} =$ 366
gate capacitance	$0.5 \cdot 0.25$	-	$C_g =$ 863	
metal-1 to substrate	$0.4 \cdot 15$	$2 \cdot 15$	1344	
metal-1 to metal-2	$68\% \cdot 0.4 \cdot 15$		156	$C_{route} =$ 1500

$$C_{qa} = C_{qd} = C_{n1} + C_{p1} + C_g + 2C_{route} = 4.88 fF \qquad (3)$$

$$C_{qb} = C_{qc} = C_{qe} = C_{qf} = C_{qk} = C_{q2} = C_{q3} = C_{q4} = C_{q5} = C_{q7} = C_{n3} = 417 aF \qquad (4)$$

$$C_{qg} = C_{qh} = C_{qj} = C_{q6} = C_{p3} = 366 aF \qquad (5)$$

$$C_{qi} = C_{q1} = C_{n1} + C_{p1} + 2C_g + 3C_{route} = 7.24 fF \qquad (6)$$

$$C_f = C_{f^\times} = C_{n1} + C_{p1} + C_{route} + C_L = 5.52 fF \qquad (7)$$

Calculation of the worst-case t_{dr}: The RC-model in Figure 3.a (Figure 3.c) expresses the charging of f ($f^\times$), assuming that the latch stores the value 0 prior to the shift. Using the Penfield-Rubinstein model, the RC equivalents yields

$$t_{dr}(f) \approx R_p \cdot (C_{qj} + 2C_f + 2C_{qk}) = 3.4 \cdot 12.2\text{ps} = \underline{\underline{43\text{ps}}} \qquad (8)$$

$$\begin{aligned} t_{dr}(f^\times) &\approx R_n \cdot (C_{q5} + 2C_{q4} + 3C_{q3} + 4C_{q2} + 5C_{q1}) + R_p \cdot (C_{q6} + 2C_{f^\times} + 2C_{q7}) \\ &= (0.78 \cdot 40.4 + 3.4 \cdot 12.2)\text{ps} = \underline{\underline{74\text{ps}}} \end{aligned} \qquad (9)$$

Calculation of the worst-case t_{df}: The RC-model in Figure 3.d (Figure 3.b) expresses the discharging of f ($f^\times$), assuming that the latch stores the value 1 prior to the shift. Using the Penfield-Rubinstein model, the RC equivalents yields

$$\begin{aligned} t_{df}(f) &\approx R_n \cdot (C_{qc} + 2C_{qb} + 3C_{qa}) + R_p \cdot (C_{qg} + 2C_{qh} + 3C_{qi}) + R_n \cdot (C_{qk} + 2C_f + 2C_{qj}) \\ &= (0.78 \cdot 6.13 + 3.4 \cdot 22.8 + 0.78 \cdot 11.8)\text{ps} = \underline{\underline{92\text{ps}}} \end{aligned} \qquad (10)$$

$$t_{df}(f^\times) \approx R_n \cdot (C_{q7} + 2C_f + 2C_{q6}) = 0.78 \cdot 12.2\text{ps} = \underline{\underline{9.5\text{ps}}} \qquad (11)$$

Comparing these delays shows that $t_{dr}(f) > t_{df}(f^\times)$ and $t_{dr}(f^\times) > t_{df}(f)$, i.e. $f^\times$ is a faster implementation of the function than f.

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Question 2.3

The dynamic power dissipation, P_{d}, accounts for the charging and discharging of the internal load capacitances, C_i:

$$P_{\mathrm{d}} = \sum(A_i \cdot C_i) \cdot V_{dd}^2 \cdot f$$

$V_{dd}^2 \cdot f$ is readily determined from the text, and relevant internal capacitances are determined above.

The nodal contribution to the dynamic power dissipation involves consideration of the fractions of patterns charging and discharging the node under consideration, i.e. the activity. In this solution, the nodal activity is approximated merely by the fraction of patterns that allow for recharging the nodes, not taking into account that an ordering of these patterns might yield a different result. Thus, the problem is reduced to determining the nodel activities, A_i, of each internal node.

The output latch changes state in 1 out of the 16 different input combinations, i.e. the nodal activity is $A_\ell = \frac{1}{16}$. The shifted capacitance is $C_\ell = (C_{qj} + C_f + C_{qk})$. This part of the power consumption is common to both circuits:

$$P_{d,\ell} = A_\ell \cdot C_\ell \cdot V_{dd}^2 \cdot f = 0.0625 \cdot 6.30fF \cdot (3V)^2 \cdot 250MHz = 0.89nW \quad (12)$$

The transistor branch Na-Nb-Nc consists of 3 nodes with nodal activities $\frac{1}{4}$, $\frac{1}{2}$, and $\frac{1}{4}$, respectively. The contribution of branch Nd-Ne-Nf is identical:

$$P_{d,abc} = (0.25 \cdot C_{qa} + 0.5 \cdot C_{qb} + 0.25 \cdot C_{qc}) \cdot (3V)^2 \cdot 250MHz = 3.45\mu W \quad (13)$$

The transistor branch Pg-Ph-Pi consists of 3 nodes with nodal activities $\frac{1}{4}$, $\frac{1}{2}$, and $\frac{1}{4}$, respectively:

$$P_{d,ghi} = (0.25 \cdot C_{qg} + 0.5 \cdot C_{qh} + 0.25 \cdot C_{qi}) \cdot (3V)^2 \cdot 250MHz = 4.69\mu W \quad (14)$$

The transistor branch N1-N2-N3-N4-N5 consists of 5 nodes with nodal activities $\frac{1}{16}$, $\frac{1}{8}$, $\frac{1}{4}$, $\frac{1}{8}$, and $\frac{1}{16}$, respectively:

$$\begin{aligned} P_{d,1-5} &= (0.0625 \cdot C_{q1} + 0.125 \cdot C_{q2} + 0.25 \cdot C_{q3} + 0.125 \cdot C_{q4} + \\ &\quad 0.0625 \cdot C_{q5}) \cdot (3V)^2 \cdot 250MHz = 1.55\mu W \end{aligned} \quad (15)$$

The dynamic power consumptions for each circuit are

$$\begin{aligned} P_{d,\mathrm{A}} &= P_{d,abc} + P_{d,def} + P_{d,ghi} + P_{d,\ell} \\ &= (2 \cdot 3.45 + 4.69 + 0.89)\mu W = \underline{\underline{12.5\mu W}} \end{aligned} \quad (16)$$

$$\begin{aligned} P_{d,\mathrm{B}} &= P_{d,1-5} + P_{d,\ell} \\ &= (1.55 + 0.89)\mu W = \underline{\underline{2.44\mu W}} \end{aligned} \quad (17)$$

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