Written test on 11^{th} January 2001

Course: Design of Integrated Circuits 1 Course no. 49260

Permitted aids: Any

Weighting: All questions are weighted equally.

A 0.25μm process is used in all problems. Geometrical design rules, list of symbols used as well as electrical parameters for the process is found in Appendix 1 on Page 5. The parameters in Appendix 1 should be used, unless the text specifies otherwise.

Problem 1

In this problem, a static combinational CMOS circuit is constructed, which realizes the function

$$Y = \overline{A \cdot B + A \cdot C \cdot D + A \cdot C \cdot E \cdot F + A \cdot C \cdot E \cdot G}$$

Question 1.1

Write down the pull-up and pull-down graphs for the function, in which both n-channel and p-channel areas can be realized as single lines of diffusion.
Draw a transistor circuit realizing the function.

Question 1.2

Draw a draft layout corresponding to the graphs above.
Calculate the dimensions of the surrounding boundary box, when minimum design rules are used.

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Problem 2

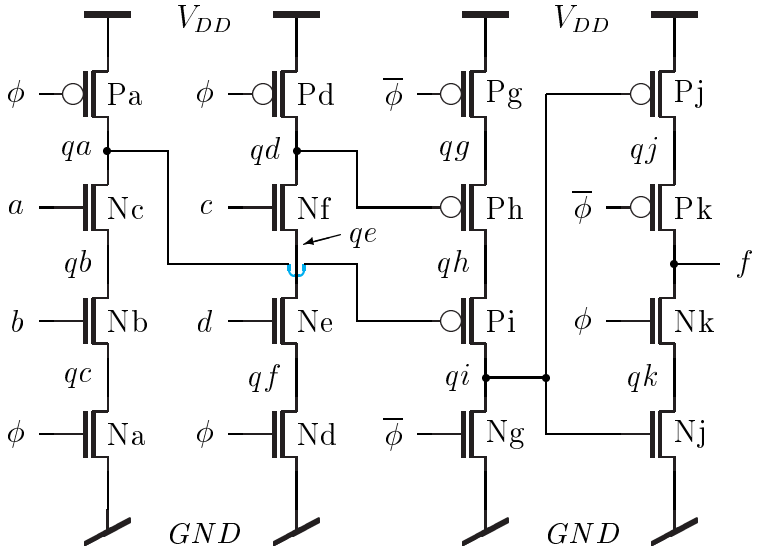

Figure 1.a: Realization 'A'

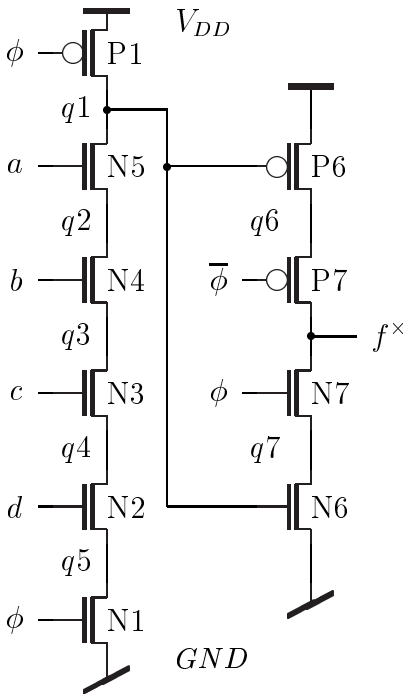

Figure 1.b: Realization 'B'

In Figures 1.a and 1.b, the transistor diagrams of two dynamic CMOS circuits are shown. In the diagrams, ϕ denotes the clock, while a, b, c, and d are inputs to the circuits.

Question 2.1

Explain, how the circuit in Figure 1.a works. Show that the circuits in Figures 1.a and 1.b realize the same function, and write down the function realized.
Describe the temporal requirements on the inputs a, b, c, and d.

In the layout, minimal geometries are used. The transistor sizes are (W,L)=(0.50μm,0.25μm). The supply voltage is $V_{DD} = 3V$. The clock frequency is $250MHz$.
The effective resistance of a transistor is $R_n = 780\Omega$ and $R_p = 3.4k\Omega$, respectively. Internal routing capacitances between two connected points are approximated by a 15μm long metal-1 wire over substrate. 68% of the area of the metal-1 wire is covered by metal-2. The output load on f or $f^{\times}$, is an additional $3fF$.

Question 2.2

Draw RC-models of the circuits for calculation of the worst-case delays t_{dr} and t_{df}, which may occur during a logic shift of the output f and $f^{\times}$.
Calculate the worst-case delays t_{dr} and t_{df} for each of the two circuits.

Question 2.3

Estimate the dynamic power consumption for each of the circuits under the assumption that, on the average, every input combination occurs equally frequently.

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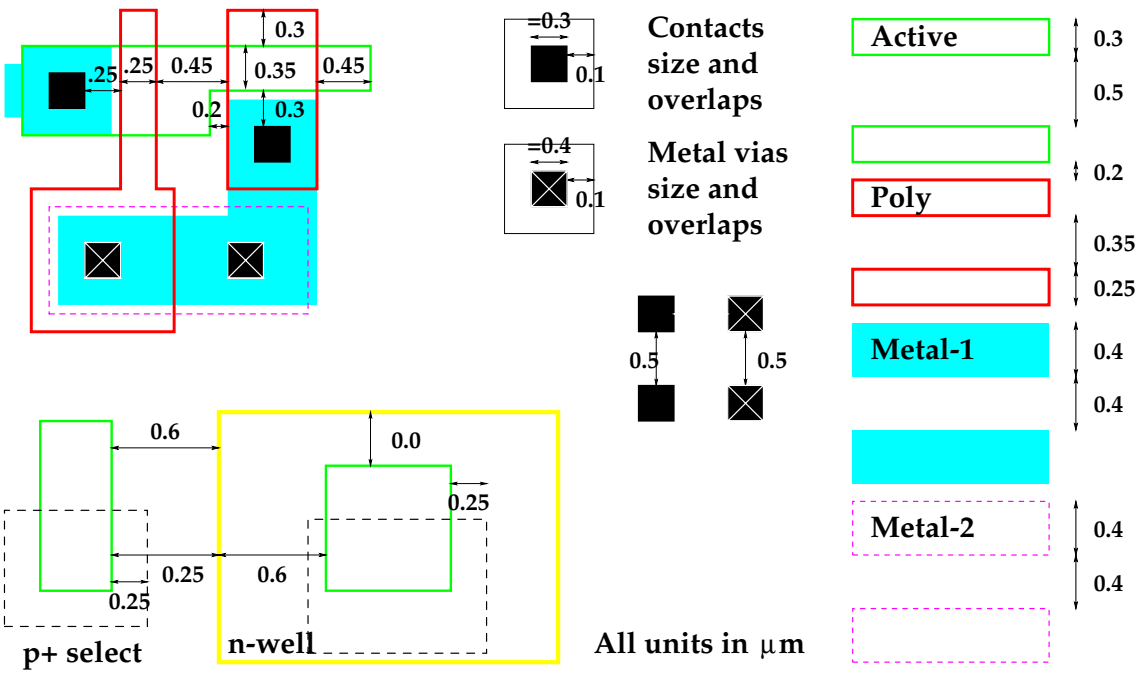
Appendix 1: 0.25μm CMOS process parameters and design rules

Transistor parameters		
Current factor $[\mu A/V^2]$	KP_n	263
	KP_p	60
Threshold voltage $[V]$	V_{tn0}	0.56
	V_{tp0}	- 0.55
Body effect coefficient $[\sqrt{V}]$	γ_n	0.336
	γ_p	0.695
Bulk potential $[V]$	ϕ_{bn}	0.323
	ϕ_{bp}	- 0.323
Channel length modulation $[V^{-1}]$	λ_n	0.010
	λ_p	0.046

Physical parameters		
Relative permittivity of oxide $[-]$	ϵ_r	3.9

Film thickness		
Gate oxide thickness	t_{ox}	50 Å
Field oxide thickness	t_F	3500 Å
Oxide thickness between poly and metal-1	t_{mp}	8000 Å
Oxide thickness between two metal layers	t_{mm}	9000 Å
Thickness of polysilicon layer	t_p	2000 Å
Thickness of any metal layer	t_m	6200 Å

Capacitances		Area $aF/\mu m^2$		Perimeter $aF/\mu m$	
metal-3	to substrate	C_{m3}	7.4	C_{m3p}	30
metal-2	to substrate	C_{m2}	11.5	C_{m2p}	34
metal-1	to substrate	C_{m1}	23.9	C_{m1p}	40
poly (on field oxide)	to substrate	C_p	88.6	C_{pp}	42
n^+ diffusion (0V)	to substrate	C_{jna}	690	C_{jnp}	138
p^+ diffusion (0V)	to substrate	C_{jpa}	596	C_{jpp}	122
gate capacitance		C_{ox}	6900	—	

In the diagram below, an excerpt of the geometrical design rules are shown. All sizes given are minimum sizes, except for contacts and metal vias, which are only sizes.