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CURRICULUM VITAE

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CURRENT POSITION

Associate professor (Danish: *"Lektor"*) at the Department of Computer Science and Applied Mathematics, Technical University of Denmark.

EDUCATION

- **Ph.D. in Engineering,** September 1999.
  University of California, Irvine, USA.
- **M.S. in Electrical and Computer Engineering,** June 1995.
  University of California, Irvine, USA.
- **Eng. Degree *"Laurea"* in Electrical Engineering,** May 1988.
  University of Rome "La Sapienza", Roma, Italy.

EXPERIENCE

- **DTU Compute, Technical University of Denmark**, Kongens Lyngby, Denmark.
  Associate professor (May '03 - current).
- **Dept. of Electrical Engineering, University of Rome "Tor Vergata"**, Rome, Italy.
  Post-doc Researcher (Sept.'99 - May '03).
- **Dept. of Electrical & Computer Engineering, University of California**, Irvine, USA.
  Research Assistant (Jan.'94 - June'99)
- **Rockwell International, Multimedia Communications Division**, Newport Beach, USA.
  Summer Intern (July'95 - Sept.'95)
- **Ericsson Telecomunicazioni**, Rome, Italy.
  System & Software Engineer (Sept.'91 - Aug.'93)
- **STMicroelectronics** (formerly SGS-Thomson Microelectronics), Agrate Brianza, Italy.
  Design Engineer (Apr.'90 - Aug.'91)
- **Military Service in the Italian Army** (Mar.'89 - Mar.'90)
- **I.P.I.A. High School**, Orvieto, Italy.
  Teacher of digital and analog electronics. (Sept.'88 - Mar.'89)

RESEARCH AREAS

Machine Learning and Approximate Computing

Approximate computing is a promising approach to energy-efficient design of digital systems in many domains such as Machine Learning (ML). The use of specialized data formats in Deep Neural Networks (DNNs), the dominant Machine Learning algorithm, could allow substantial improvements in processing time and power efficiency.

In this line of research, we are focusing on applying variable precision formats, called Tunable Floating-Point (TFP), to ML algorithms. The TFP novelty is flexibility that allows to set different precisions for different operations and to tune the precision of given layers of the neural network to obtain higher power efficiency.

Internet-of-Things and Edge Computing

Increasingly sophisticated and computationally intensive algorithms are required for applications running on mobile devices and embedded processors constituting the Internet-of-Things (IoT). These applications include audio and image recognition, machine learning, and security. Today, heavy computations are transferred to servers (the cloud), but in the paradigm of "Edge" computing, it is desirable to perform the computation locally to decrease latency, network traffic and reduce the overall energy footprint.

In this context, this line of reseach focuses on the design of Application Specific Processors (ASPs) to accelerate software applications in portable systems and at the Edge. We opted to implement the ASPs in FPGAs, because FPGA-based accelerators can be designed and fine tuned to match exactly the algorithm, and FPGAs can be reconfigured at run-time by making the system adaptable to the specific workload.

Energy Efficient Computation

The main objective of this traditional line of research is to reduce the power dissipation in digital processors without penalizing the performance with the objective of reducing the computation energy footprint and increasing the system's reliability. Emphasis is given to the more frequent and challenging arithmetic operations.

TEACHING DUTIES

Years 2003-(today)

Courses currently taught at the **Technical University of Denmark**.

- *VLSI Design*, M.S. level course, from 2004–*current*.
- *Computer Architecture*, B.S. level course, from 2009–*current*.
- *Design of Arithmetic Processors*, M.S. level course, introduced in 2007, from 2007–*current*.

Courses discontinued or not taught anymore at **Technical University of Denmark**

- *Advanced Digital Design Techniques*, M.S. level course, introduced in 2004 and discontinued in 2011.
- *Digital Systems*, B.S. level course, taught in 2004 and 2005.

Years 1999-2003

- **University of Rome "Tor Vergata"**, Roma, Italy
  - *Digital Electronics* (Italian: *"Elettronica digitale"*), Academic Years 2000/01 and 2001/02.
  - *Signal Processing in Measurement Systems* (Italian: *"Elaborazione dei segnali di misura"*), Academic Years 2000/01, 2001/02, 2002/03.
- **University of Perugia**, Orvieto campus, Italy
  - *Design of Data Acquisition and Processing Systems* (Italian: *"Sistemi di acquisizione ed elaborazione"*), Academic Years 1999/2000, 2000/01, 2001/02, 2002/03.
  - *Electronic Instruments and Measurement* (Italian: *"Misure elettroniche"*), Academic Year 2000/01.

Previous years

- **Dept. of Electrical & Computer Eng., University of California**, Irvine (USA)
  Teaching Assistant (1994 - 1999)

OTHER ACTIVITIES

- Steering Committee Board member *IEEE Symposium on Computer Arithmetic*, 2015–2018
- Member of the IEEE Computer Society Technical Meeting Request Committee (TMRC), 2013–*current*.
- Associate Editor for *IEEE Transactions on Computers*, 2011–2016.
- Associate Editor for *IET Computers and Digital Techniques* , 2012–2016.
- Program Co-Chair for the *21st IEEE Symposium on Computer Arithmetic*, April 2013.
- Program Committee member of several international conferences.
- Reviewer for several conferences and journals.

SUMMARY OF PUBLICATIONS

	Quantity
Refereed international journals	10
Refereed proceedings of international conferences	73
Book chapters	6
Other publications	12

Indices from **Google Scholar** (23/03/2018) – http://scholar.google.dk/citations?user=anannarelli

citations	1200
h-index	18
i10-index	33

LIST OF PUBLICATIONS

Journal Articles (Peer Review)

[1] E. Antelo, P. Montuschi, and **A. Nannarelli**. "Improved 64-bit Radix-16 Booth Multiplier Based on Partial Product Array Height Reduction", *IEEE Transactions on Circuits and Systems I*, vol. 64, n. 2, pp. 409-418, Feb. 2017.
Journal's Impact Factor: 2.823 *(Source: 2017 Journal Citation Reports by Clarivate Analytics, 2018)*

[2] **A. Nannarelli**. "Performance/Power Space Exploration for Binary64 Division Units", *IEEE Transactions on Computers*, vol. 65, n. 5, pp. 1671-1677, May 2016.
Journal's Impact Factor: 2.916 *(Source: 2016 Journal Citation Reports by Thomson Reuters, 2017)*

[3] A. T. Winther, W. Liu, **A. Nannarelli**, and S. Vrudhula. "Thermal Aware Floorplanning Incorporating Temperature Dependent Wire Delay Estimation", *Microprocessors and Microsystems*, vol. 39, n. 8, pp. 807-815, Nov. 2015.
Journal's Impact Factor: 0.471 *(Source: 2015 Journal Citation Reports by Thomson Reuters, 2016)*

[4] W. Liu, A. Calimera, A. Macii, E. Macii, **A. Nannarelli**, and M. Poncino. "Layout-Driven Post-Placement Techniques for Temperature Reduction and Thermal Gradient Minimization", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 32, no. 3, pp. 406-418, Mar. 2013.

[5] T. Lang and **A. Nannarelli**. "Comments on 'Improving the Speed of Decimal Division", *IET Computers and Digital Techniques*, vol. 6, no. 6, pp. 370-371, 2012.

[6] W. Liu and **A. Nannarelli**. "Power Efficient Division and Square Root Unit", *IEEE Transactions on Computers*, vol. 61, no. 8, pp. 1059-1070, Aug. 2012.

[7] T. Lang and **A. Nannarelli**. "A Radix-10 Digit-Recurrence Division Unit: Algorithm and Architecture", *IEEE Transactions on Computers*, June 2007. Vol. 56(6), p. 727-739, June 2007.

[8] E. Antelo, T. Lang, P. Montuschi, and **A. Nannarelli**. "Digit-Recurrence Dividers with Reduced Logical Depth", *IEEE Transactions on Computers*, Vol. 54, p. 837-851, July 2005.

[9] L. Benini, A. Macii, and **A. Nannarelli**. "A Code Compression Architecture for Cache Energy Minimization in Embedded Systems", *IEE Proceedings - Computers and Digital Techniques. Special Issue on Low-Power Systems-on-Chip*. Vol. 149, Iss. 4, p. 157-163, July 2002.

[10] **A. Nannarelli** and T. Lang. "Low-Power Divider", *IEEE Transactions on Computers*, Vol. 48, p. 2-14, Jan. 1999.

Conference Papers (Peer Review)

[1] M. Franceschi, **A. Nannarelli** and M. Valle, "Tunable Floating-Point for Artificial Neural Networks", *Proc. of 25th IEEE International Conference on Electronics Circuits and Systems (ICECS 2018)*, p. 289-292. Bordeaux, France, Dec. 2018.

[2] G.C. Cardarilli, L. Di Nunzio, R. Fazzolari, **A. Nannarelli**, and M. Re, "A Power Efficient Digital Front-End for Cognitive Radio Systems", *Proc. of 52nd Asilomar Conference on Signals, Systems, and Computers*, p. 199-202. Pacific Grove (CA), USA, Nov. 2016.

[3] M. Franceschi, **A. Nannarelli** and M. Valle, "Tunable Floating-Point for Embedded Machine Learning Algorithms Implementation", *Proc. of 15th Int.l Conf. on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)*, p. 89-92. Prague, Czech Republic. July 2018.

[4] G. C. Cardarilli, L. Di Nunzio, R. Fazzolari, M. Matta, M. Re, **A. Nannarelli**, D. Gelfusa, S. Lorenzo and S. Spanó, "Digital Architecture and ASIC Implementation of Wideband Delta DOR Spacecraft Onboard Tracker", *Proc. of 15th Int.l Conf. on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)*, p. 17-20. Prague, Czech Republic. July 2018.

[5] **A. Nannarelli**. "Tunable Floating-Point for Energy Efficient Accelerators", *Proc. of 25th IEEE Symposium on Computer Arithmetic*, p. 29-36, Amherst, USA. 25-27 June 2018.

[6] **A. Nannarelli**. "A Multi-Format Floating-Point Multiplier for Power-Efficient Operations", *Proc. of the 30th IEEE Int.l System-on-Chip Conference*, p. 351-356. Munich, Germany. Sep. 2017.

[7] **A. Nannarelli**, M. Re, G.C. Cardarilli, L. Di Nunzio, M. Spaziani Brunella, R. Fazzolari and F. Carbonari. "Robust Throughput Boosting for Low Latency Dynamic Partial Reconfiguration", *Proc. of the 30th IEEE Int.l System-on-Chip Conference*, p. 86-90. Munich, Germany. Sep. 2017.

[8] A. Lomuscio, G.C. Cardarilli, **A. Nannarelli**, and M. Re, "A Hardware Framework for on-Chip FPGA Acceleration", *International Symposium on Integrated Circuits (ISIC 2016)*. Accepted. Dec. 2016.

[9] A. Esposito, A. Lomuscio, G.C. Cardarilli, L. Di Nunzio, R. Fazzolari, **A. Nannarelli**, and M. Re, "Dynamically-Loaded Hardware Libraries (HLL) Technology for Audio Applications", *Proc. of 50th Asilomar Conference on Signals, Systems, and Computers*. Pacific Grove (CA), USA, Nov. 2016.

[10] J. Taylor and **A. Nannarelli**, "Design and Simulation of a Quaternary Memory Cell based on a Physical Memristor", Proc. of 2016 IEEE Nordic Circuits and Systems Conference (NorCAS), Copenhagen, Denmark. Nov. 2016,

[11] G.C. Cardarilli, L. Di Carlo, **A. Nannarelli**, F. M. Pandolfi, and M. Re, "A Framework for Dynamically-Loaded Hardware Library (HLL) in FPGA Acceleration", *Proc. of IEEE International Symposium on Signal Processing and Information Technology (ISSPIT)*, Abu Dhabi, UAE, Dec. 2015

[12] **A. Nannarelli** , "Reliability in Warehouse-Scale Computing: Why Low Latency Matters", *Proc. of MEDIAN Finale, Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale*, Tallinn, Estonia, Nov. 2015.

[13] G.C. Cardarilli, **A. Nannarelli**, M. Petricca, and M. Re, "Characterization of RNS multiply-add units for power efficient DSP", *Proc. of 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Fort Collins, Colorado (USA), Aug. 2015.

[14] P. Albicocco, G. C. Cardarilli, **A. Nannarelli**, and M. Re, "Twenty Years of Research on RNS for DSP: Lessons Learned and Future Perspectives", *Proc. of the International Symposium on Integrated Circuits (ISIC 2014)*, Singapore, Dec. 2014.

[15] J.K. Toft and **A. Nannarelli**, "Energy Efficient FPGA based Hardware Accelerators for Financial Applications", *Proc. of the 32nd Norchip Conference*, Tampere, Finland. Oct. 2014.

[16] **A. Nannarelli**, "Decimal Engine for Energy-Efficient Multicore Processors", *Proc. of the 22nd International Conference on Very Large Scale Integration (VLSI-SoC)*, Playa del Carmen, Mexico, Oct. 2014.

[17] P. Albicocco, G. C. Cardarilli, **A. Nannarelli**, M. Petricca, and M. Re, "Truncated Multipliers through Power-Gating for Degrading Precision Arithmetic", *Proc. of 47th Asilomar Conference on Signals, Systems, and Computers*. pp. 2172-2176, Pacific Grove (CA), USA, Nov. 2013.

[18] J. S. Hegner, J. Sindholt, and **A. Nannarelli**, "Design of Power Efficient FPGA based Hardware Accelerators for Financial Applications", in *Proc. of the 30th Norchip Conference*, Copenhagen, Denmark, Nov. 2012.

[19] P. Albicocco, G. C. Cardarilli, **A. Nannarelli**, M. Petricca, and M. Re, "Imprecise Arithmetic for Low Power Image Processing", *Proc. of 46th Asilomar Conference on Signals, Systems, and Computers*, pp. 983-987, Pacific Grove (CA), USA, Nov. 2012.

[20] M. Petricca, P. Albicocco, G. C. Cardarilli, **A. Nannarelli**, and M. Re, "Power Efficient Design of Parallel/Serial FIR Filters in RNS", in *Proc. of 46th Asilomar Conference on Signals, Systems, and Computers*, pp. 1015-1019, Pacific Grove (CA), USA, Nov. 2012.

[21] A. Calimera, W. Liu, E. Macii, **A. Nannarelli**, and M. Poncino, "Power and Aging Characterization of Digital FIR Filters Architectures", *Proc. of the First Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale (MEDIAN'12)*, Annecy, France, June 2012.

[22] **A. Nannarelli**, "FPGA Based Acceleration of Decimal Operations", *Proc. of International Conference on ReConFigurable Computing and FPGA's* , p. 146–151, Cancun, Mexico. 30 Nov.–2 Dec. 2011.

[23] A. T. Winther, W. Liu, **A. Nannarelli**, and S. Vrudhula, "Temperature Dependent Wire Delay Estimation in Floorplanning", *Proc. of 2011 Norchip Conference*, Lund, Sweden, 14–15 Nov. 2011.

[24] N. Borup, J. Dindrop, and **A. Nannarelli**, "FPGA Implementation of Decimal Processors for Hardware Acceleration", *Proc. of 2011 Norchip Conference*, Lund, Sweden, 14–15 Nov. 2011.

[25] P. Albicocco, G.C. Cardarilli, **A. Nannarelli**, M. Petricca, and M. Re, "Degrading precision arithmetics for low-power FIR implementation", *Proc. of 2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Seoul, South Korea, 7-10 Aug. 2011.

[26] **A. Nannarelli**, "Radix-16 Combined Division and Square Root Unit", *Proc. of 20th IEEE Symposium on Computer Arithmetic*, p. 169–176, Tubingen, Germany, 25–27 July 2011.

[27] W. Liu and **A. Nannarelli**, "Temperature Aware Power Optimization for Multicore Floating-Point Units", *Proc. of 44th Asilomar Conference on Signals, Systems, and Computers*, p. 1134-1138, Pacific Grove (CA), USA, Nov. 2010.

[28] G.C. Cardarilli, **A. Nannarelli**, Y. Oster, M. Petricca, and M. Re, "Design of Large Polyphase Filters in the Quadratic Residue Number System", *Proc. of 44th Asilomar Conference on Signals, Systems, and Computers*, p. 410-413, Pacific Grove (CA), USA, Nov. 2010.

[29] M. Petricca, G.C. Cardarilli, **A. Nannarelli**, M. Re, and P. Albicocco, "Degrading Precision Arithmetic for Low Power Signal Processing", *Proc. of 44th Asilomar Conference on Signals, Systems, and Computers*, p. 1163-1167, Pacific Grove (CA), USA, Nov. 2010.

[30] W. Liu and **A. Nannarelli**, "Power Dissipation Challenges in Multicore Floating-Point Units", *Proc. of 21st IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP 2010)*, p. 257-264, Rennes, France, July 2010.

[31] W. Liu, A. Calimera, **A. Nannarelli**, E. Macii, and M. Poncino, "Post-placement Temperature Reduction Techniques", *Proc. of 2010 Design Automation and Test in Europe Conference (DATE 2010)*, p. 634-637, Dresden, Germany, Mar. 2010.

[32] S. Gonzalez-Navarro, **A. Nannarelli**, C. Tsen, and M. J. Schulte, "Combined Decimal and Binary Floating-point Divider", *Proc. of 43rd Asilomar Conference on Signals, Systems, and Computers*, p. 930-934, Pacific Grove (CA), USA, Nov. 2009.

[33] M. Petricca, H. Li, S. Forchhammer, **A. Nannarelli**, M. Re, J. D. Andersen, and G.C. Cardarilli, "Hardware Implementation of Real-Time MPEG Analysis and Deblocking for Video Enhancement", *Proc. of 43rd Asilomar Conference on Signals, Systems, and Computers*, p. 754-758, Pacific Grove (CA), USA, Nov. 2009.

[34] I. Shuli, M. Petricca, G.C. Cardarilli, **A. Nannarelli**, and M. Re, "Multiple Constant Multiplication through Residue Number System", *Proc. of 43rd Asilomar Conference on Signals, Systems, and Computers*, p. 736-739, Pacific Grove (CA), USA, Nov. 2009.

[35] **A. Nannarelli**, "Low Power Hardware Platforms", *Proc. of 12th International Symposium on Wireless Personal Multimedia Communications (WPMC'09)*, Sendai, Japan. Sep. 7-10, 2009.

[36] W. Liu, A. Calimera, **A. Nannarelli**, E. Macii, and M. Poncino, "On-chip Thermal Modeling Based on SPICE Simulation", *Proc. of 19th International Workshop on Power And Timing Modeling, Optimization and Simulation PATMOS 2009*, p. 66-75. Delft, Netherlands, Sep. 2009.

[37] T. Lang and **A. Nannarelli**, "Division Unit for Binary Integer Decimals", *Proc. of 20th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP '09)*, p. 1-7, Boston, USA, 7-9 July 2009.

[38] W. Liu and **A. Nannarelli**, "Net Balanced Floorplanning Based on Elastic Energy Model", *Proc. of 26th Norchip Conference*, p. 258-263, Tallinn, Estonia, Nov. 2008.

[39] W. Liu and **A. Nannarelli**, "Power Dissipation in Division", *Proc. of 42nd Asilomar Conference on Signals, Systems, and Computers*, p. 1790-1794, Pacific Grove (CA), USA, Oct. 2008.

[40] **A. Nannarelli**, M. Re, and G.C. Cardarilli, "Reducing Power Dissipation in Pipelined Accumulators", *Proc. of 42nd Asilomar Conference on Signals, Systems, and Computers*, p. 2098-2101, Pacific Grove (CA), USA, Oct. 2008.

[41] G.C. Cardarilli, **A. Nannarelli**, and M. Re, "On the Comparison of Different Number Systems in the Implementation of Complex FIR Filters", *Proc. of 16th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, p. 37-41, Rhodes, Greece, Oct. 2008.

[42] L. Dadda and **A. Nannarelli**, "A Variant of a Radix-10 Combinational Multiplier", *Proc. of 2008 IEEE International Symposium on Circuits and Systems (ISCAS)*, p. 3370-3373, Seattle, USA, May 18-21, 2008.

[43] G.C. Cardarilli, L. Di Nunzio, **A. Nannarelli**, and M. Re. "ADAPTO: Full-Adder Based Reconfigurable Architecture for Bit Level Operations", *Proc. of 2008 IEEE International Symposium on Circuits and Systems (ISCAS)*, p. 3434-3437, Seattle, USA, May 18-21, 2008.

[44] G.C. Cardarilli, **A. Nannarelli**, and M. Re, "Residue Number System for Low Power DSP Applications", *Proc. of 41st Asilomar Conference on Signals, Systems, and Computers*, p. 1412-1416, Pacific Grove (CA), USA, Nov. 4-7, 2007.

[45] G.C. Cardarilli, A. Del Re, **A. Nannarelli**, and M. Re, "Impact of RNS Coding Overhead on FIR Filters Performance", *Proc. of 41st Asilomar Conference on Signals, Systems, and Computers*, p. 1426-1429, Pacific Grove (CA), USA, Nov. 4-7, 2007.

[46] T. Lang and **A. Nannarelli**, "Combined radix-10 and radix-16 division unit", *Proc. of 41st Asilomar Conference on Signals, Systems, and Computers*, p. 967-971, Pacific Grove (CA), USA, Nov. 4-7, 2007.

[47] G.L. Bernocchi, G.C. Cardarilli, A. Del Re, **A. Nannarelli**, and M. Re, "Low-power adaptive filter based on RNS components", *Proc. of 2007 IEEE International Symposium on Circuits and Systems (ISCAS)*, p. 3211-3214, New Orleans, USA, May 28-31, 2007

[48] T. Lang and **A. Nannarelli**, "A Radix-10 Combinational Multiplier", *Proc. of 40th Asilomar Conference on Signals, Systems, and Computers*, p. 313-317, Pacific Grove (CA), USA, Oct. 29 – Nov. 1, 2006.

[49] **A. Nannarelli**, M.S. Rasmussen, and M.B. Stuart, "A 1.5 GFLOPS Reciprocal Unit for Computer Graphics", *Proc. of 40th Asilomar Conference on Signals, Systems, and Computers*, p. 1682-1686, Pacific Grove (CA), USA, Oct. 29 – Nov. 1, 2006.

[50] G.L. Bernocchi, G.C. Cardarilli, A. Del Re, **A. Nannarelli**, and M. Re. "A hybrid RNS adaptive filter for channel equalization", *Proc. of 40th Asilomar Conference on Signals, Systems, and Computers*, p. 1706-1710, Pacific Grove (CA), USA, Oct. 29 – Nov. 1, 2006.

[51] G.C. Cardarilli, A. Del Re, **A. Nannarelli**, and M. Re, "Low Power and Low Leakage Implementation of RNS FIR Filters", *Proc. of 39th Asilomar Conference on Signals, Systems, and Computers*, p. 1620-1624, Pacific Grove (CA), USA, Oct. 30 – Nov. 2, 2005.

[52] E. Antelo, T. Lang, P. Montuschi, and **A. Nannarelli**, "Low Latency Digit-Recurrence Reciprocal and Square-Root Reciprocal Algorithm and Architecture", *Proc. of 17th Symposium on Computer Arithmetic*, p. 147-152, Cape Cod, USA, June 27-29, 2005.

[53] G.C. Cardarilli, A. Del Re, **A. Nannarelli**, and M. Re, "Programmable Power-of-two RNS Scaler and its Application to a QRNS Polyphase Filter", *Proc. of 2005 IEEE International Symposium on Circuits and Systems (ISCAS)*, p. 1002-1005, Kobe, Japan, May 23-26, 2005.

[54] G.C. Cardarilli, A. Del Re, **A. Nannarelli**, and M. Re, "Low-Power Implementation of Polyphase Filters in Quadratic Residue Number System", *Proc. of 2004 IEEE International Symposium on Circuits and Systems* (ISCAS), Vol. II, p. 725-728, May 23-26, 2004.

[55] A. Del Re, **A. Nannarelli**, and M. Re, "A tool for automatic generation of RTL-level VHDL description of RNS FIR filters", *Proc. of 2004 Design, Automation and Test in Europe Conference* (DATE), Vol. 48, p. 686-687, Paris, France, Feb. 16-20, 2004.

[56] **A. Nannarelli**, G.C. Cardarilli, and M. Re, "Power-delay tradeoffs in residue number system", *Proc. of 2003 IEEE International Symposium on Circuits and Systems* (ISCAS), Vol. V, p. 413-416, May 25-28, 2003.

[57] G.C. Cardarilli, A. Del Re, R. Lojacono, **A. Nannarelli**, and M. Re, "RNS implementation of high performance filters for satellite demultiplexing", *Proc. of the 2003 IEEE Aerospace Conference*, Vol. 3, p. 1365-1379, Mar. 8-15, 2003.

[58] E. Antelo, T. Lang, P. Montuschi, and **A. Nannarelli**, "Fast Radix-4 Retimed Division with Selection by Comparisons", *Proc. of IEEE 13th International Conference on Application-specific Systems, Architectures and Processors (ASAP 2002)*, p. 185-196, San Jose (CA), USA, July 17-19, 2002.

[59] G.C. Cardarilli, A. Del Re, **A. Nannarelli**, and M. Re, "Residue Number System Reconfigurable Datapath", *Proc. of 2002 IEEE International Symposium on Circuits and Systems* (ISCAS), Vol. II, p. 756-759, Phoenix, Arizona, USA, May 2002.

[60] G.C. Cardarilli, A. Del Re, **A. Nannarelli**, and M. Re, "Power Characterization of Digital Filters Implemented on FPGA", *Proc. of 2002 IEEE International Symposium on Circuits and Systems* (ISCAS), Vol. V, p. 801-804, Phoenix, Arizona, USA, May 2002.

[61] A. Del Re, **A. Nannarelli**, and M. Re, "Implementation of Digital Filters in Carry-Save Residue Number System", *Proc. of 35th Asilomar Conference on Signals, Systems, and Computers*, p. 1309-1313, Pacific Grove (CA), USA, Nov. 2001.

[62] A. Del Re, **A. Nannarelli**, and M. Re, "Fast Prototyping Techniques Applied to the Hardware Simulation of Telecommunication Systems", *Proc. of 35th Asilomar Conference on Signals, Systems, and Computers*, p. 1314-1317, Pacific Grove (CA), USA, Nov. 2001.

[63] **A. Nannarelli**, M. Re, A. Del Re, G.C. Cardarilli, and R. Lojacono, "High Speed RNS A/D Front End", *Proc. of 6th Euro Workshop on ADC Modelling and Testing*, p. 19-22, Lisbona, Portugal, Sep. 2001.

[64] L. Benini, A. Macii, and **A. Nannarelli**, "Cached-Code Compression for Energy Minimization in Embedded Processors", *Proc. of International Symposium on Low Power Electronics and Design (ISLPED)*, p. 322-327, Huntington Beach, California, USA, Aug. 2001.

[65] **A. Nannarelli**, M. Re, and G.C. Cardarilli, "Tradeoffs between Residue Number System and Traditional FIR Filters", *Proc. of IEEE International Symposium on Circuits and Systems* (ISCAS), Vol. II, p. 305-308, Sydney, Australia, May 2001.

[66] M. Re, **A. Nannarelli**, G.C. Cardarilli, and R. Lojacono, "FPGA Implementation of RNS to Binary Signed Conversion Architecture", *Proc. of IEEE International Symposium on Circuits and Systems* (ISCAS), Vol. IV, p. 350-353, Sydney, Australia, May 2001.

[67] A. D'Amora, **A. Nannarelli**, M. Re, and G.C. Cardarilli, "Reducing Power Dissipation in Complex Digital Filters by using the Quadratic Residue Number System", *Proc. of 34th Asilomar Conference on Signals, Systems, and Computers*, p. 879-883, Pacific Grove (CA), USA, Nov. 2000.

[68] G.C. Cardarilli, **A. Nannarelli**, and M. Re, "Reducing Power Dissipation in FIR Filters using the Residue Number System", *Proc. of 43rd IEEE Midwest Symposium on Circuits and Systems*, p. 320-323, Lansing, USA, Aug. 2000.

[69] **A. Nannarelli** and T. Lang, "Low-Power Radix-4 Combined Division and Square Root", *Proc. of IEEE International Conference on Computer Design* (ICCD), p. 236-242, Austin, Texas, USA, Oct. 1999.

[70] **A. Nannarelli** and T. Lang, "Low-Power Division: Comparison among implementations of radix 4, 8 and 16". *Proc. of 14th Symposium on Computer Arithmetic*, p. 60-67, Adelaide, Australia, Apr. 1999.

[71] **A. Nannarelli** and T. Lang, "Low-Power Radix-8 Divider", *Proc. of IEEE International Conference on Computer Design* (ICCD), p. 420-426, Austin, Texas, USA, Oct. 1998.

[72] **A. Nannarelli** and T. Lang, "Power-Delay Tradeoffs for Radix-4 and Radix-8 Dividers", *Proc. of International Symposium on Low Power Electronics and Design* (ISLPED), p. 109-111, Monterey, California, USA, Aug. 1998.

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Book Chapters

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