POWER EVALUATION TOOL : modeling and implementation

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Abstract

The objective of the work is to develop a software tool to rapidly evaluate the power consumption of a CMOS circuit realized with standard cells. This tool, simulation based, is intended to be used in designing low-power arithmetic units and provide a reliable and fast procedure to compare power dissipation among different schemes and implementations. This tool, which we called **PET**: power evaluation tool, consists of three C routines that interact with the COMPASS tools and provides accurate evaluations with a small time overhead.

1 Introduction

The objective of the work is to develop a software tool to rapidly evaluate the power consumption of a CMOS circuit realized with standard cells. This tool, simulation based, is intended to be used in designing low-power arithmetic units and provide a reliable and fast procedure to compare power dissipation among different schemes and implementations.

2 Power Dissipation

The relationship between power and energy dissipated in a clock cycle is :

$$Power = Energy\ per\ cycle \times frequency \qquad [Watt].$$

The power consumption in a cell is proportional to the output load and to the frequency of the switching [1].

$$P = \left({V_{DD}}^2 C_L + E^{INT}\right) f \qquad [Watt]$$

$$E = {V_{DD}}^2 C_L + E^{INT} \qquad [Joule]$$

where:

V_{DD} is power supply voltage.

C_L is the total load applied to the output.

E^{INT} is the internal energy dissipated in the cell during one transition.

f is the frequency (cell's output switching rate).

In the sequential cells also the internal switching, not affecting the cell's output, dissipates power. To take into account this contribution we can write the power expression in the following way:

$$P = (E^{INT} + {V_{DD}}^2 C_L) f_{out} + E^{cl} f_{cl} \qquad [Watt]$$

where :

f_{out} is the output switching rate.

f_{cl} is the frequency of the cell's clock.

E^{cl} is the energy dissipation per clock cycle when output doesn't switch.

E^{INT} is the additional part of the energy dissipated when the output changes.

Now we consider a large circuit containing N cells both combinational and sequential. The total power consumption is given by:

$$P_{TOT} = \sum_{i=1}^{N} P_i = \sum_{i=0}^{N} f_i E_i \qquad [Watt]$$

where :

f_i is the switching frequency of the i-cell.

E_i is the energy per cycle of the i-cell.

Introducing an activity factor a_i defined as

$$a_i = \frac{f_i}{f_o} = \frac{i-cell\ nr.\ of\ output\ transitions}{clock\ nr.\ of\ transitions}$$

and being f_o the circuit main frequency (clock frequency), we can write:

$$P_{TOT} = f_o \sum_{i=0}^{N} E_i a_i$$

and remembering the expression for E_i

$$P_{TOT} = f_o \sum_{i=0}^{N} a_i ({E_i}^{INT} + {V_{DD}}^2 C_{Li})$$

If N_S is the number of sequential cells, the power consumption expression becomes

$$P_{TOT} = f_0 \sum_{i=1}^{N} ({E_i}^{INT} + {V_{DD}}^2 C_{Li}) {a_i}^{out} +$$

$$f_0 \sum_{i=1}^{N_S} {E_i}^{cl} {a_i}^{cl} \qquad [Watt]$$

where :

${a_i}^{out} = \frac{f_{out,i}}{f_0}$ is the output activity coefficient of i-cell.

${a_i}^{cl} = \frac{f_{cl,i}}{f_0}$ is the i-cell clock input activity coefficient. This is the most general case in which the i-cell clock rate might be different from f_0.

Using the number of transitions in place of the frequencies

$$P_{TOT} = \frac{f_0}{n_0} \sum_{i=1}^{N} ({E_i}^{INT} + {V_{DD}}^2 C_{Li}) {n_i}^{out} +$$

$$\frac{f_0}{n_0} \sum_{i=1}^{N_S} {E_i}^{cl} {n_i}^{cl} \qquad [Watt] \quad (I)$$

3 Procedure

In order to to calculate the power dissipated, given by equation (I), we need to determine the value of the parameters indicated.

V_{DD} is the power supply voltage.

f_0 is the clock frequency.

n_0 is the number of clock transitions in the time window we are considering

${n_i}^{out}$ is the number of transitions seen at the output of the i-cell.

${n_i}^{cl}$ is the number of the clock transitions seen at the input of the sequential i-cell.

C_{Li} is the load at the output of the i-cell.

${E_i}^{INT}$ is the energy per transition dissipated inside the i-cell.

${E_i}^{cl}$ is the energy dissipated in the sequential i-cell every time the clock input changes.

The quantities V_{DD}, E^{INT} and E^{cl} depend on the library that we are using. C_L depends on the layout (topology, type of cell connected and wire capacitance) we are designing and all the n quantities depend again on the layout and on the set of input vectors we are using. The procedure can be summarized by the following steps:

1. For the chosen library determine the quantities E^{INT} and E^{cl} for each cell. These values can be provided directly by the silicon vendors.
2. From the layout, extract the capacitance at each node and associate them as output load (C_L) to each cell.
3. Choose a set of test vectors and run a simulation using a tool that is able to detect transition (i.e. a logical level simulator)
4. Calculate the power using expression (I).

4 Implementation

The procedure described above was implemented in the tool we called **PET**: power evaluation tool. It consist of three C routines (**analyze**, **ttgen** and **calpot**) and the use of the two COMPASS tools **sim** (Mixed-Mode simulator) and **extract** (COMPASS Interconnect layout to netlist extractor) [2]. The latter is used to determine the capacitance (including wires) at each node of the circuit while **sim** is used to determine the logic values of the nodes used later to determine the number of transitions. The structure of the tool can be seen in Figure 1. A description of **PET** is given in the following sections.

4.1 analyze

analyze reads the extracted netlist and determines the output load for each cell of the circuit. It also provides to **sim** the labels of the nodes to monitor. The files read are:

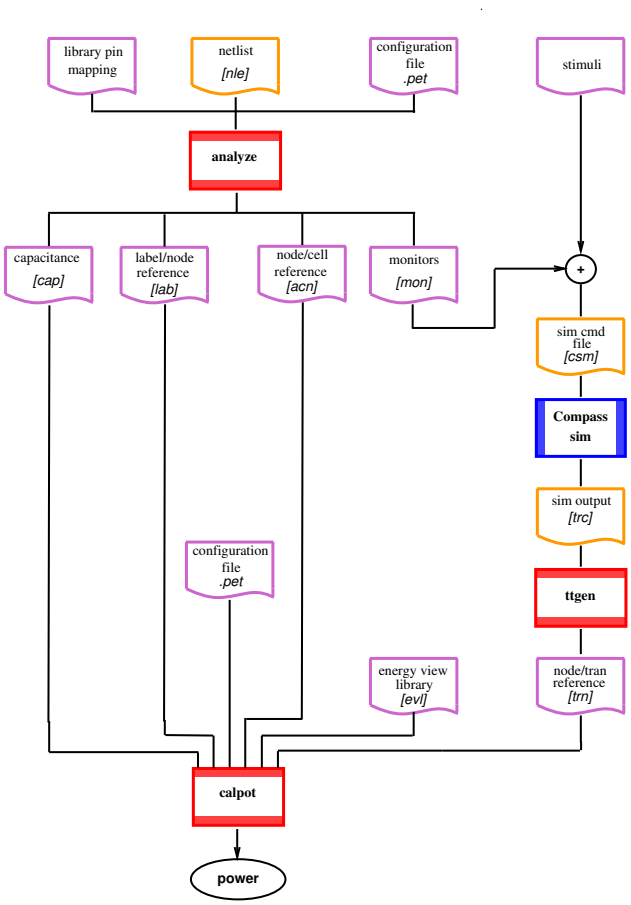

Figure 1: Structure of PET

- a configuration file containing general parameters such as: power supply voltage (V_{DD}), clock frequency, time window of the simulation, reference to the standard cells library.
- the netlist [nle] extracted by **extract**.
- a file containing the mapping of cell's pins for the library. It is needed to associate the capacitance of node x to the output of cell i.

The files produced are:

- a list of the nodes (file [mon]) to be monitored by **sim**.
- the reference capacitance-node (file [cap]).
- the reference cell's output-node (file [acn]).
- the reference label-node (file [lab]).

All these references are resolved later by **calpot**.

After we have generated the [mon] file, adding the input stimuli to that, we create a COMPASS [csm] command file ready to be used along with the netlist [nle] in **sim**.

4.2 ttgen

sim generates a simulation output file [trc] in tabular format. **ttgen** (transitions table generator) reads this file and create a transitions table [trn]. In this table each label/node is associated with the number of transitions occurred at that node during the simulation.

4.3 calpot

Finally **calpot** calculates the power dissipation according to (I). The files read are:

- the three files generated by **analyze**: [cap], [acn], [lab].
- the transitions table file [trn] produced by **ttgen**.
- the configuration file containing library parameters.
- a file containing the values E^{INT} and E^{cl} for each cell of the library.

Power dissipation is given in mW.

5 Operating Procedure

We can now summarize the steps to do when using **PET**.

1. Make sure that the values E^{INT} and E^{cl} are stored in the library file. If some value is missing determine it by using an electrical level simulator (i.e. spice).
2. Design the circuit and generate the layout.
3. Extract the netlist using **extract**.
4. Run **analyze** on the extracted netlist [nle].
5. Put together the input stimuli and file [mon] in the COMPASS command file [csm].
6. Run **sim** and obtain file [trc].
7. Use **ttgen** to generate file [trn].
8. Run **calpot** to calculate the power dissipation.

6 Experimental Results

PET was used on some test circuits to determine its accuracy and reliability. The test was carried out comparing the results obtained by **PET** with those obtained using an electrical level simulator and calculating the power as the product of the voltage and the average current over a time window of the same size of that used for **PET**. Due to the large CPU time needed by **spice** to simulate a circuit containing several gates, we couldn't compare between large circuits. The difference between **PET** and **spice** was never greater than 10%.

7 Conclusions

We needed a tool to rapidly evaluate the power dissipation in a circuit to compare between different schemes. **PET** fullfills our needs by providing a good evaluation with a small time overhead. The difference between **PET** and an electrical level simulator was never greater than 10%. This result is satisfactory because we are more interested in comparing among different schemes, and evaluating the variations in the power dissipation, rather than knowing its absolute value.

REFERENCES

[1] N. H. E. Weste and K. Eshraghian. *Principles of CMOS VLSI Design*. Addison-Wesley Publishing Company, 2nd edition, 1993.

[2] Compass Design Automation. *User Manuals for COMPASS VLSI*. Compass Design Automation, Inc., 1992.

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