Intel® Xeon Phi™ Coprocessor
Highly-Parallel Processing

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Highly-Parallel Processing
*Seamlessly solves most important problems of any scale*

**Intel® Xeon Phi™ product family**
- Based on Intel® Many Integrated Core (Intel® MIC) architecture
- Leading performance for highly parallel workloads
- Common Intel® Xeon® programming model seamlessly increases developer productivity
- Launching on 22nm with >50 cores

**Intel® Xeon® processor**
- Ground-breaking real-world application performance
- Industry-leading energy efficiency
- Meet HPC challenges and scale for growth
Introducing Intel® Xeon Phi™ Coprocessors

Highly-parallel Processing for Unparalleled Discovery

**Groundbreaking Differences**

- Up to 61 IA cores/1.1 GHz/ 244 Threads
- Up to 8GB memory with up to 352 GB/s bandwidth
- 512-bit SIMD instructions; fma
- Linux operating system, IP addressable
- Standard programming languages and tools

**Leading to Groundbreaking Results**

- Up to 1 TeraFlop/s double precision peak performance\(^1\)
- Up to 2.2x higher memory bandwidth than on an Intel® Xeon® processor E5 family-based server.\(^2\)
- Up to 4x more performance per watt than with an Intel® Xeon® processor E5 family-based server.\(^3\)

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products.

For more information go to [http://www.intel.com/performance](http://www.intel.com/performance). Notes 1, 2 & 3, see backup for system configuration details.
Intel® Xeon Phi™ Coprocessors Much More Than That

General purpose IA Hardware leads to less idle time for your investment.

Restrictive architectures

- Operate as a compute node
- Run a full OS
- Program to MPI
- Run x86 code
- Run offloaded code

It’s a supercomputer on a chip

Custom HW Acceleration

- Run restricted code

Intel® Xeon Phi™ Coprocessor

Restrictive architectures limit the ability for applications to use arbitrary nested parallelism, functions calls and threading models.

Source: Intel Estimates
Shipping in 2012
*Intel® Xeon Phi™ Coprocessor 5110P*

**Performance**

- Up to 1 TFLOP of double-precision (peak)

**Programmability**

- C, C++, Fortran
- Intel and 3rd party tools

**Applications**

- Memory Bandwidth / Capacity Bound workloads
- Ideal for:
  - Molecular Modeling,
  - Digital Content Creation,
  - and Energy

Ideal for memory bandwidth and memory capacity bound workloads

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Shipping in 2013
*Intel® Xeon Phi™ Coprocessor 3100 Product Family*

**Performance**

- Up to 1 TFLOP of double-precision (peak)\(^1\)
- 6GB GDDR5
- 240 GB/s Bandwidth
- Active and passive form factors at 300W TDP

**Programmability**

- C, C++, Fortran
- Intel and 3\(^{rd}\) party tools

**Applications**

- Compute Bound workloads
- Ideal for MonteCarlo, Black-Scholes, Life Sciences

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Ideal for compute bound workloads

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\(^1\) Claim based on calculated theoretical peak double precision performance capability for a single 3100 family coprocessor = 1.0032 TeraFlop/s.
Intel® Xeon Phi™ Coprocessor: Increases Application Performance up to 10x

Application Performance Examples

<table>
<thead>
<tr>
<th>Customer</th>
<th>Application</th>
<th>Performance Increase^1 vs. 2S Xeon*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Los Alamos</td>
<td>Molecular Dynamics</td>
<td>Up to 2.52x</td>
</tr>
<tr>
<td>Acceleware</td>
<td>8th order isotropic variable velocity</td>
<td>Up to 2.05x</td>
</tr>
<tr>
<td>Jefferson Labs</td>
<td>Lattice QCD</td>
<td>Up to 2.27x</td>
</tr>
<tr>
<td>Financial</td>
<td>BlackScholes SP Monte Carlo SP</td>
<td>Up to 7x</td>
</tr>
<tr>
<td>Labs</td>
<td>Up to 10.75x</td>
<td></td>
</tr>
<tr>
<td>Sinopec</td>
<td>Seismic Imaging</td>
<td>Up to 2.53x^2</td>
</tr>
<tr>
<td>Sandia Labs</td>
<td>miniFE (Finite Element Solver)</td>
<td>Up to 2x^3</td>
</tr>
<tr>
<td>Intel Labs</td>
<td>Ray Tracing (incoherent rays)</td>
<td>Up to 1.88x^4</td>
</tr>
</tbody>
</table>

* Xeon = Intel® Xeon® processor;
* Xeon Phi = Intel® Xeon Phi™ coprocessor

Notes:
1. 2S Xeon* vs. 1 Xeon Phi* (preproduction HW/SW & Application running 100% on coprocessor unless otherwise noted)
2. 2S Xeon* vs. 2S Xeon* + 2 Xeon Phi* (offload)
3. 8 node cluster, each node with 2S Xeon* (comparison is cluster performance with and without 1 Xeon Phi* per node) (Hetero)

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For more information go to [http://www.intel.com/performance](http://www.intel.com/performance)
Synthetic Benchmark Summary (Intel® MKL) (5110P)

SGEMM (GF/s)

Up to 2.7X
Higher is Better

1,729

DGEMM (GF/s)

Up to 2.7X
Higher is Better

833

SMP Linpack (GF/s)

Up to 2.3X
Higher is Better

722

STREAM Triad (GB/s)

Up to 2.1X
Higher is Better

171

Notes

1. Intel® Xeon® Processor E5-2670 used for all SGEMM Matrix = 13824 x 13824, DGEMM Matrix 7936 x 7936, SMP Linpack Matrix 30720 x 30720
2. Intel® Xeon Phi™ coprocessor 5110P (ECC on) with “Gold Release Candidate” SW stack SGEMM Matrix = 11264 x 11264, DGEMM Matrix 7680 x 7680, SMP Linpack Matrix 26872 x 28672

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1. Peak DP FLOPS claim based on calculated theoretical peak double precision performance capability for a single coprocessor. 16 DP FLOPS/clock/core * 60 cores * 1.053GHz = 1.0108 TeraFlop/s.

2. Memory Bandwidth: 2 socket Intel® Xeon® processor E5-2600 product family server vs. Intel® Xeon Phi™ coprocessor (2.2x: Measured by Intel October 2012. 2 socket E5-2670 (8 core, 2.6GHz) vs. 1 Intel® Xeon Phi™ coprocessor SE10P (61 cores, 1.1GHz) on STREAM Triad benchmark 79.5 GB/s vs. 175GB/s ) (TR 2012B)

3. Performance/Watt: 2 socket Intel® Xeon® processor E5-2670 server vs. a single Intel® Xeon Phi™ coprocessor SE10P (Intel Measured DGEMM perf/watt score 309 GF/s @ 335W vs. 829 GF/s @ 195W) (TR 2028B)